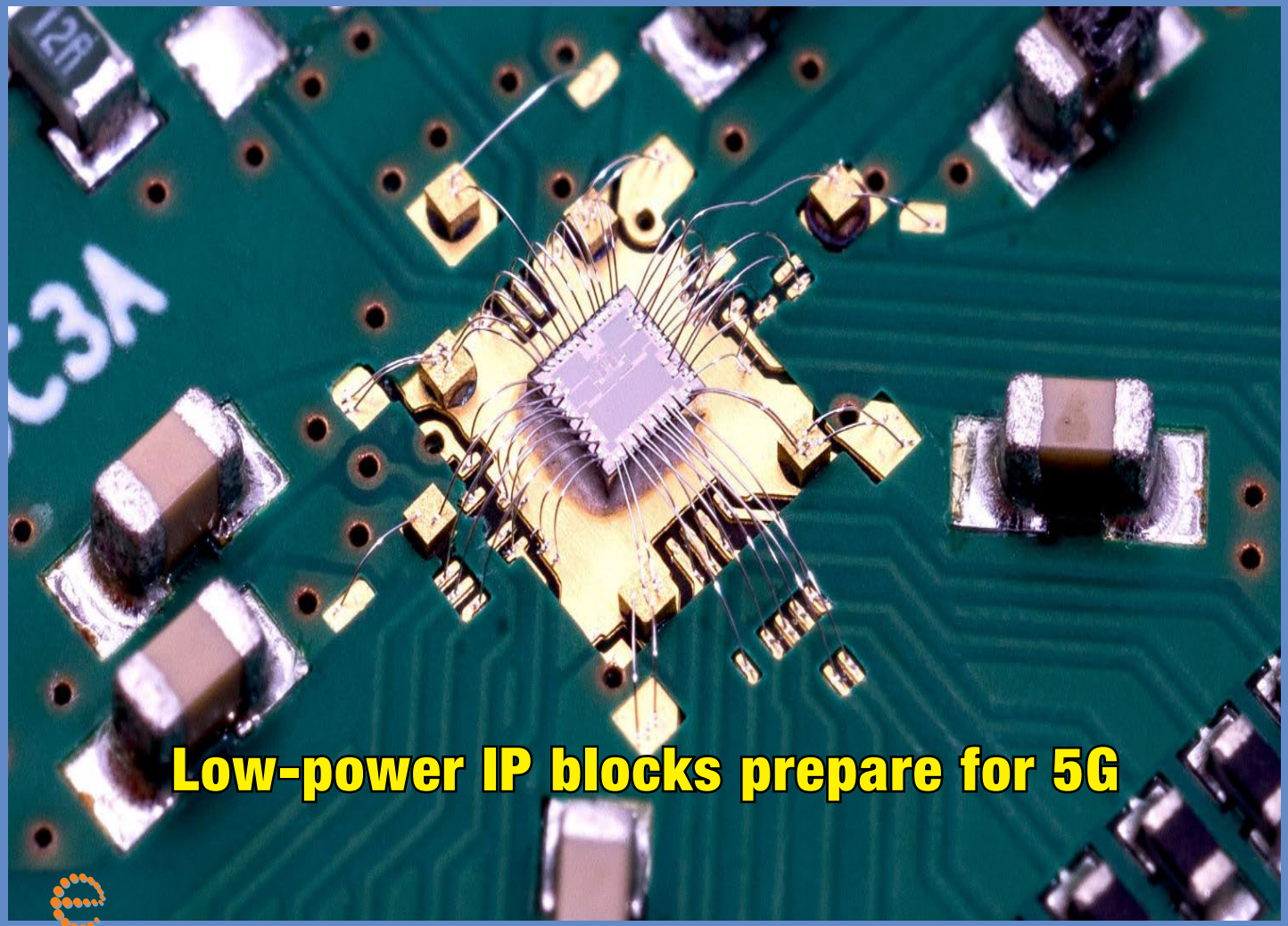
SEPTEMBER 2017

eeDesignNews

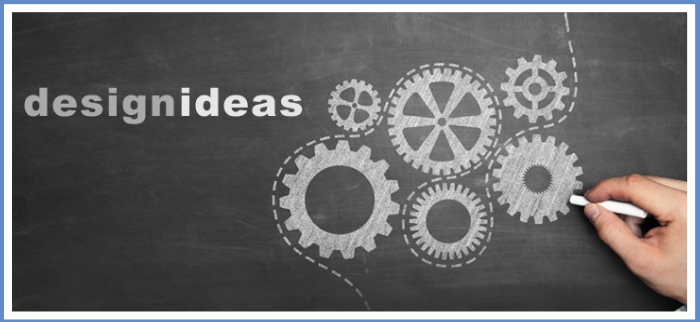
www.eedesignnewseurope.com

electronics europe Design

europe



Low-power IP blocks prepare for 5G

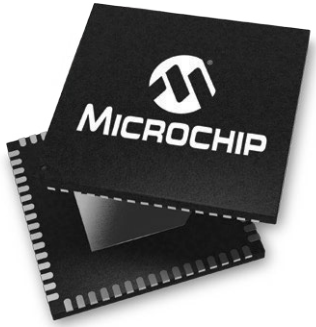


european business press

Scalable Automotive Network Solutions

Cost-Efficient • Real-Time • Flexible

Microchip has been delivering robust, automotive-qualified CAN, LIN, Ethernet, MOST® technology and USB solutions to automotive suppliers for over ten years. Our MOST technology and USB solutions are the de facto standards for in-vehicle infotainment and consumer device connectivity worldwide. If your automotive design requires in-vehicle transport of audio, video, control or Ethernet packet data, we offer solutions which work reliably over UTP, coax and optical physical layers with guaranteed low latency. Software stacks are also available from Microchip, as well as third parties, allowing you to focus your efforts on application software development.



Application Examples

- Body control
- LTE/3G connectivity
- Ambient LED lighting
- Rear-view camera
- HMI
- Exterior LED lighting
- Top-view camera
- Infotainment head unit
- Smart sensors

microchip DIRECT
www.microchipdirect.com

MICROCHIP

www.microchip.com/automotive

COVER

ADC, RF-FE, low-power IP blocks for 5G comms

Belgium-based nano-electronics and digital technology research body imec has disclosed details of two key building blocks (as IP) for future 5G applications featuring record low power consumption; an ADC and a 60-GHz RF front-end.

The first IP block is a fast and compact successive approximation analogue-to-digital converter, for smartphone applications in the below-6GHz band; the compact, low-cost, low-power and high-speed (300 Msample/sec) ADC (pictured on the cover page) meets the requirements of multimode multiband 5G communication. The ADC has a reduced core area of 350 x 325 µm when fabricated in 16-nm CMOS. It achieves a dynamic low power consumption of 3.6 mW at 300 Msample/sec and low-frequency signal to noise and distortion ratio (SNDR) of 70.2 dB at 204 Msample/sec.

The compact, energy efficient and low-cost radio front-end (TRX) operates at 60GHz. The chip features 8-way calibration-free beamforming at RF frequencies to support a large number of antennas, making the technology attractive for fixed wireless access and small cell backhaul. The on-chip transmit-receive switching allows sharing of the antenna array between transmit and receive mode. The 9.6 mm^2 chip is implemented in 28 nm CMOS and consumes 231 mW in receive and 508 mW in transmit mode (0.9V supply). Full item here.

FEATUREARTICLES

ONLINE THIS MONTH

Motor-driver IC PCB layout guidelines (Part 1)

Motor-driver IC PCB layout guidelines, Part 2

Interview: Refined ReRAM enters the storage wars

Over-the-air BLE test systems solve wireless quality issues

Virtualised ECUs with Renesas R-Car: new challenges and opportunities

Prevent overloads with safety capacitors: a 12-point checklist

eeDn's columns

Can we do better?

by Graham Prophet, Editor

I am often asked why I harbour a certain amount of negative sentiment about the software design process. A simplistic answer might be; look at the big picture; consider the plethora of tools, analysis software, and checkers of all sorts that are on offer in the market. Any process which requires that much inspection and rectification to reach its goals must have a question mark against its fitness for purpose.

Contrast the process within the hardware domain. We have been designing ICs for about as long as we have been working with compiled language computing. Faced with the consequences of Moore's Law, EDA has evolved a hierarchical approach that abstracts the design activity away from the low-level detail, and that makes (some sort of) an attempt at correct-by-construction flow. It's still a long, long way from flawless algorithm-in/geometry-out, but it at least has aspirations in that direction. Coding, by contrast, has gone almost nowhere; the Fortran writer of 1957 would find much of C, 60 years later, immediately familiar. (C++, to be fair, might take him/her a day or two.)

What – you might well ask – would a more optimum flow look like? I imagine something like this (which I recognise is hopelessly idealised);

Step 1 - write the architectural description in plain language, followed by a long period of contemplation and consideration of whether that description correctly captures the design intent. Step 2 - transfer that into a format that still looks and reads like plain language, but with a restricted vocabulary in which every terms has a precise meaning: a very (very) high level programming language, if you like. From that point on, no human intervention is allowed; by however many steps it takes, and with formal verification at each stage, a hierarchy of tools would take the code to an executable form, fully automated. Changes allowed only by returning to the highest, plain-language level.

EDA offers the user an unspoken pact. It says, "do only things that the automatics understand and can handle, and together we can crank out something that stands a chance of working."

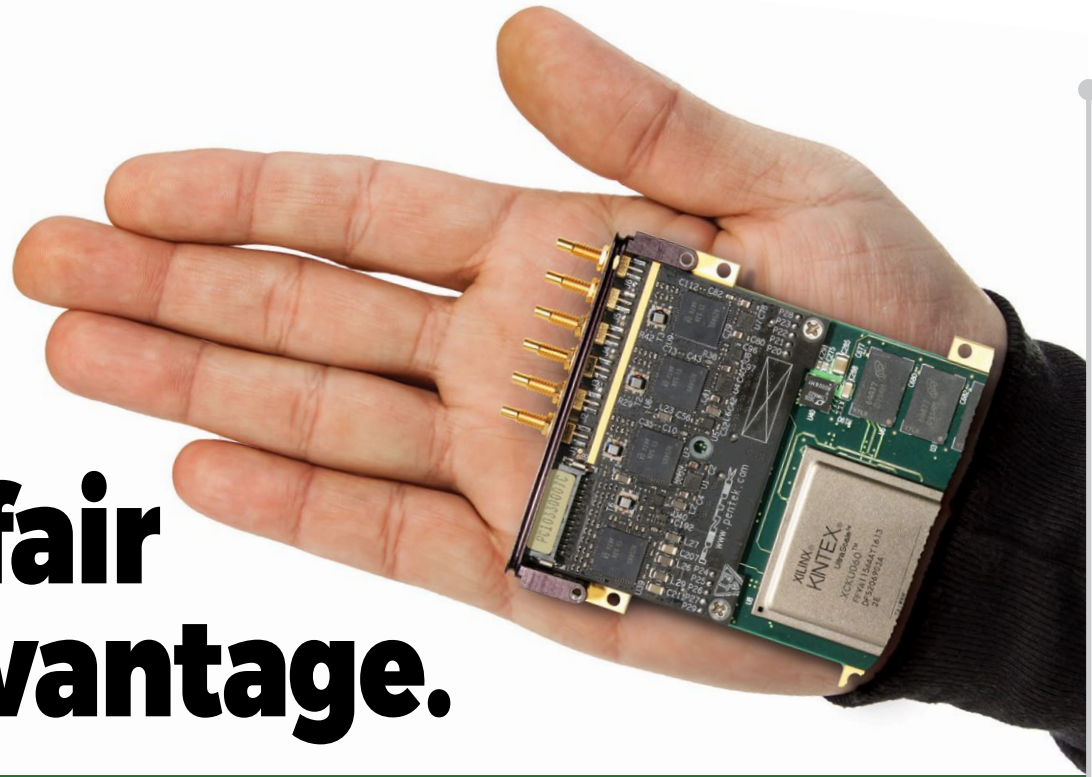
No such deal is on offer to the software coder: by contrast, the software world has prized the freedom to do anything and everything that can conceivably be coded. Which leads to the situation that, after over half a century of compiled-language computing, you cannot – in the most commonly-used language in the embedded space – tell a computing device to add two numbers without first laboriously telling it what sort of numbers they are going to be, and carefully specifying where they should be stored.

Is it appropriate to ask, "what's wrong with this picture?"

Accepting that programmers are not likely to happily accept working in a more constrained space, and as I have written here before, there is also the question of where and when the design takes place. We have always, on this publication, prized the process of design; but we have a situation where, if we are honest, we should admit that a significant proportion of software projects are hardly designed at all. They are executed ad-hoc, such design processes as do exist being carried out on-the-fly as the job proceeds. The result is then bug-fixed and massaged until it more-or-less works, and is released, with the comfort blanket that software is infinitely fixable, and there's always another release. The fact that in the IoT world fixes are even easier, as every product holds its code in flash and allows over-the-air updates, simply adds to the pressure to sign-off version 1.0 – and stores up problems for the connected world we are creating.

Right now, there is an added risk in the "teach our kids to code" movement, compounded by technically-illiterate politicians leaping on the bandwagon, with no understanding that the key engineering skills are applied more in the sitting-and-thinking phase (we used to give it labels such as 'systems analysis') than in the coding itself.

To crystallise the second of these concerns; we should be carrying out our creativity in sentences that end with a (.) Whereas we are encouraged, and even compelled, to do so in sentences that end with (;)



Unfair Advantage.

2X **HIGHER** performance | 4X **FASTER** development

Introducing Jade™ architecture and Navigator™ Design Suite, the next evolutionary standards in digital signal processing.

Pentek's new Jade architecture, based on the latest generation Xilinx® Kintex® Ultrascale™ FPGA, doubles the performance levels of previous products. Plus, Pentek's next generation Navigator FPGA Design Kit and BSP tool suite unleashes these resources to speed IP development and optimize applications.

- **Streamlined Jade architecture** boosts performance, reduces power and lowers cost
- **Superior analog and digital I/O** handle multi-channel wideband signals with highest dynamic range
- **Built-in IP functions** for DDCs, DUCs, triggering, synchronization, DMA engines and more
- **Board resources** include PCIe Gen3 x8 interface, sample clock synthesizer and 5 GB DDR4 SDRAM
- **Navigator Design Suite** BSP & FPGA Design Kit (FDK) for Xilinx Vivado® IP Integrator expedite development
- **Applications** include wideband phased array systems, communications transceivers, radar transponders, SIGINT and ELINT monitoring and EW countermeasures

All this plus FREE lifetime applications support!

PENTEK
Setting the Standard for Digital Signal Processing

Pentek, Inc., One Park Way, Upper Saddle River, NJ 07458
Phone: 201-818-5900 • Fax: 201-818-5904 • email: info@pentek.com • **www.pentek.com**

Model 71861 4-Channel 200 MHz A/D with DDC, Kintex UltraScale FPGA - XMC

JADE

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (digital downconverters)
- Optional 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2, & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Also available in VPX, cPCI and AMC with rugged options

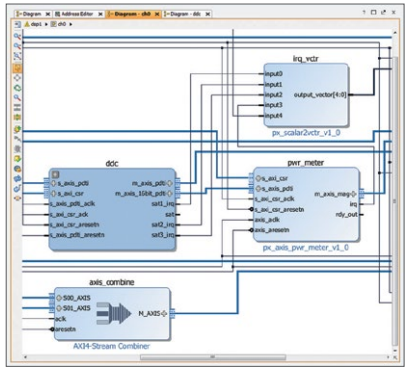
Datasheet: pentek.com/go/71861edne

NAVIGATOR
Design Suite

Pentek's Navigator Design Suite includes:

- Navigator FPGA Design Kit (FDK) for integrating custom IP into the Pentek factory-shipped design
- Navigator Board Support Package (BSP) for creating host applications

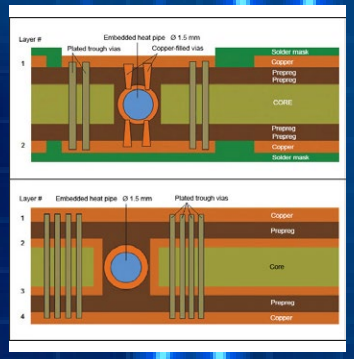
Datasheet:
pentek.com/go/navigatoredne



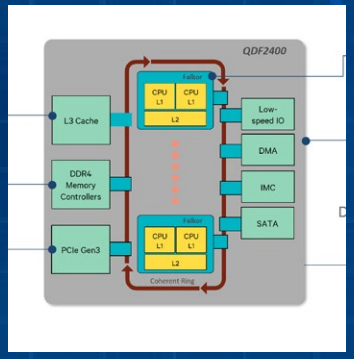
Navigator FDK shown in IP Integrator.

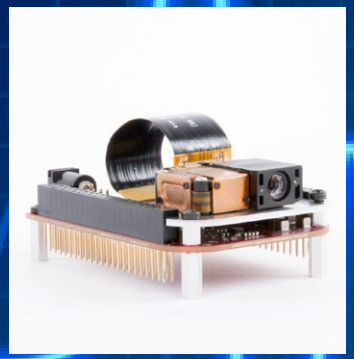
See the Video!
www.pentek.com/go/ednejade or
call 201-818-5900 for more information

pulse


Layer #
Embedded heat pipe Ø 1.5 mm
Plated trough vias
Copper-filled vias
Solder mask
Copper
Prepreg
CORE
Layer #
Embedded heat pipe Ø 1.5 mm
Plated trough vias
Copper
Prepreg
Core


MYRIAD X High Performance • Ultra-Low Power
Movidius
MA2485
Myriad X
8.7 mm
8.5 mm
Neural Com
for dedica
learnir
3rd Generati
vision processing u

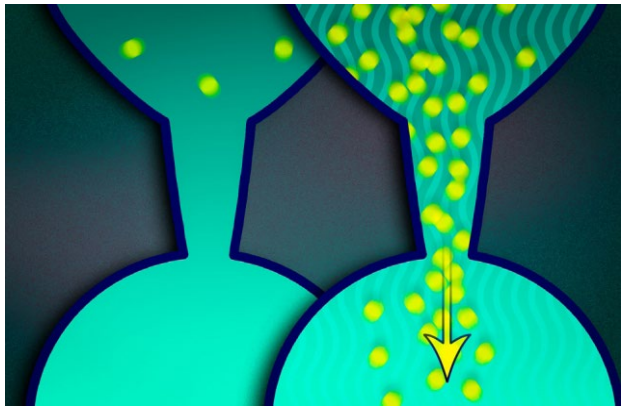

QDF2400
Falkor
CPU
L1
L2
L3 Cache
DDR4 Memory Controllers
PCIe Gen3
Low-speed IO
DMA
IMC
SATA
Coherent Ring




qorvo
5G RF

"Superballistic" electron flow verified, in graphene structures

In a paper published in the journal Nature Physics, researchers at the University of Manchester, UK, and at Massachusetts Institute of Technology (MIT) have reported physical verification of a theoretical prediction that electrons constrained to pass through a small (atomic scale) space do so faster 'en masse' than individually. The result may have implications for semiconductor device fabrication as geometries scale further from the nano to the atomic level. Behaving like particles in a viscous fluid can help 'bunches' of electrons 'squeeze' through a tight space, says the MIT report. (image above; MIT) The physical medium in which the effect was observed is graphene – a material in which the Manchester University team have been pioneers.



The theory of so-called superballistic flow predicts that electrons can pass more easily through constrictions by interacting with one another, and thereby "cooperating," than they can individually. The theory was proposed in a paper earlier in 2017 by a team led by MIT professor of physics Leonid Levitov. In this report, the team at the University of Manchester, working alongside Levitov and MIT undergraduate Haoyu Guo, have confirmed the theory in an experiment employing devices built from an atomically thin layer of graphene. Using the experimental set-up described theoretically in Levitov's previous paper, the Manchester researchers, led by professor of physics and Nobel laureate Andre Geim, carefully etched a series of constrictions, or pinch points, within pieces of graphene encapsulated between boron-nitride crystals.

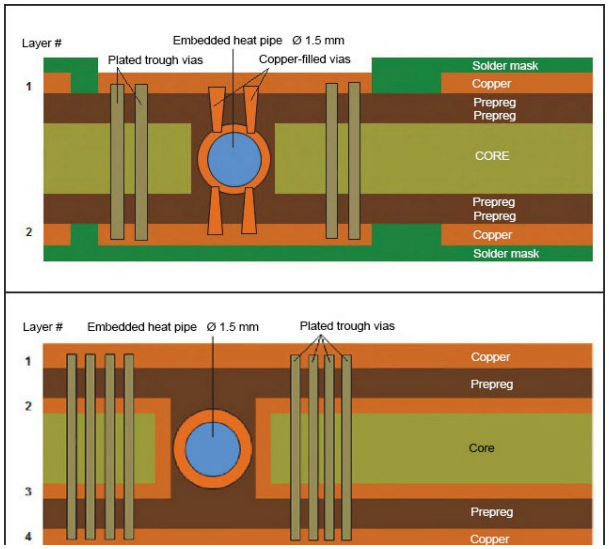
The researchers then measured the drop in electric potential over each constriction independently, allowing them to detect the flow rate through each pinch point in the device. They found that the conductance of the electrons exceeded the maximum conductance possible for free electrons, known as Landauer's ballistic limit. They also found that the conductance of the electrons increased with a rise in temperature.

Complete article, here

Heat pipes integrated in PCB layers boost thermal performance

Austrian printed-board specialist AT&S has developed the capability to embed miniature heat pipes within the layer structure of complex printed circuit boards, to more effectively transfer heat away from high-dissipation components, without the necessity to add very heavy layers of additional copper. AT&S describes the placement of the heat pipes as "embedded and inserted" in the PCB. The company notes the ever-increasing power densities of today's designs, along with the need to have products operate in environmentally-sealed housings, making heat dissipation an even more challenging task.

Thermal management in the PCB is conventionally done by adding more copper to the PCB structure with constructions such as thick copper layers, Plated Through Holes (PTHs), copper filled laser vias or even copper inlays. Such methods can provide good heat dissipation, but can be also related to some disadvantages for several reasons: in the special case of



thick copper planes for heat spreading, the production of the PCB becomes more costly and difficult since dedicated equipment to handle the heavy thick copper panels is required.

Modern heat pipes are small enough to be incorporated to PCB constructions. Their thickness can range from about 400 µm up to 2 mm. AT&S has applied expertise in embedding components, and in 2.5D technology, in order to combine mini heat pipes with the PCB. The application of heat pipes directly in the PCB body allows new design freedom such as remote cooling, heat guiding and heat spreading.

AT&S has developed a method of integrating "ready-to-use" mini heat pipes into the PCB body turning it into a complete heat management module. Various PCB demonstrator samples with embedded and inserted heat pipes have been manufactured. AT&S R&D is actively looking for partners who have special challenges regarding thermal solutions for their future products and are willing to test the HP-PCB technology as early adopters. This includes designs that are demanding in other dimensions, such as embedded components, high frequency materials, or material hybridization.

Complete article, here

Intel's Movidius Myriad X VPU hosts Neural Compute Engine, for 'AI at the Edge'

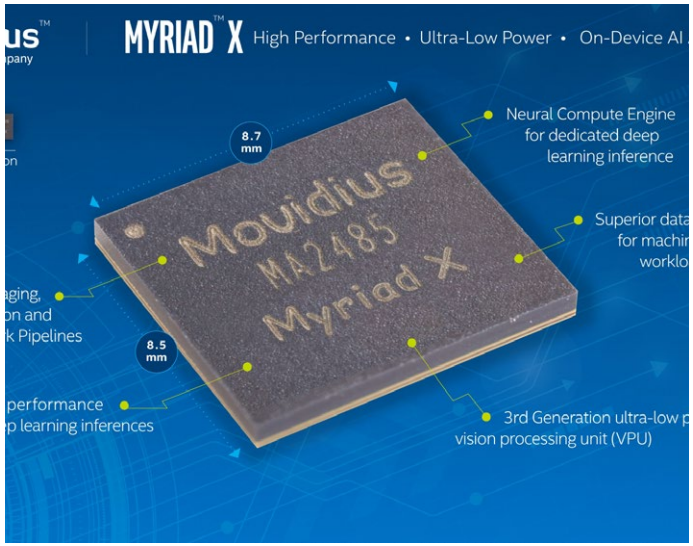
Intel's Movidius Myriad X vision processing unit (VPU) is configured to deliver more autonomous capabilities across a wide range of product categories including drones, robotics, smart cameras and virtual reality.

Myriad X is presented as the first system-on-chip (SOC) with a dedicated Neural Compute Engine for accelerating deep learning inferences at the edge. The Neural Compute Engine is an on-chip hardware block specifically designed to run deep neural networks at high speed and low power without compromising accuracy, enabling devices to see, understand and respond to their environments in real time.

Myriad X architecture is capable of 1 TOPS of compute performance on deep neural network inferences. [Intel enlarges 'TOPS' to mean 'trillion operations per second', presumed equivalent to Tera-Ops.]

"We're on the cusp of computer vision and deep learning becoming standard requirements for the billions of devices surrounding us every day," Intel comments.

Capable of delivering more than 4 TOPS of total performance (aggregated over all processing units), its form factor and on-board processing are aimed at autonomous devices. In addition to its Neural Compute Engine, Myriad X com-

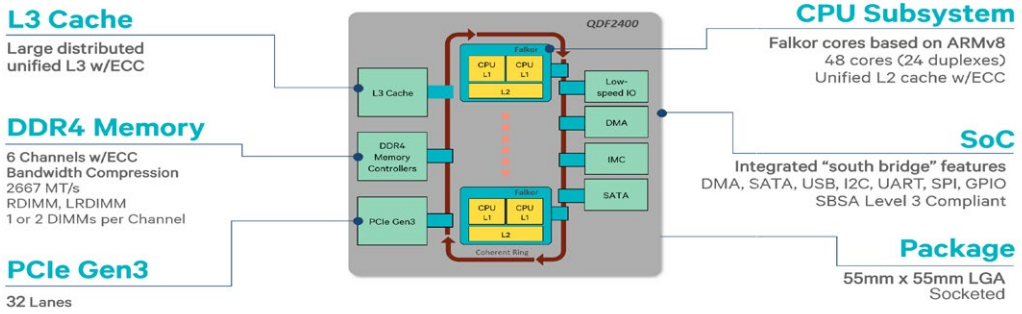


bines imaging, visual processing and deep learning inference in real time with:
- Programmable 128-bit VLIW vector processors to run multiple imaging and vision application pipelines simultaneously with the flexibility of 16 vector processors optimized for computer vision workloads.
- Increased configurable MIPI Lanes connect up to 8 HD resolution RGB cameras directly to Myriad X with its 16 MIPI lanes included in its rich set of interfaces, to support up to 700 million pixels per second of image signal processing throughput.
- Enhanced vision accelerators apply over 20 hardware accelerators to perform tasks such as optical flow and stereo depth without introducing additional compute overhead.
- 2.5 MB of homogenous on-chip memory comprises a centralized on-chip memory architecture that allows for up to 450 GB/sec of internal bandwidth, minimizing latency and reducing power consumption by minimizing off-chip data transfer.

Complete article, here

Power management is key to Qualcomm's 10nm, 48 core ARM server chip by Nick Flaherty

Power management has been a key design consideration for the industry's first 10nm 48 core ARM server chip developed by Qualcomm. Details of the Centriq 2400 system-on-chip (SoC) and its Falkor processor core were shown at the Hot Chips conference in August 2017. This is the first ARM-based server chip in 10nm, running at 2GHz from a 1.0V supply.
The Falkor core was designed from the ground up specifically for the cloud datacentre server market. The ARMv8 64bit core has two custom Falkor CPUs, a shared L2 cache and a shared bus interface to the Qualcomm System Bus (QSB) ring interconnect.
This modular building block serves as the foundation for the 48-core Centriq 2400 SoC design.
A range of power management techniques was included in the design from the start, such as independent power-state control for each of the CPUs and L2, with entry to and exit from low-power states controlled by hardware state machines for ultra-fast state transitions, and hardware state retention for power-collapsed sleep states with ultra-fast recovery.
The micro-architecture of each CPU has a 4-issue, 8-dispatch heterogeneous pipeline that is designed to optimize performance per unit of power, with variable length pipelines that are tuned per function to maximize throughput and minimize idle hardware.
It also uses out-of-order and rename resources to prevent instruction retirement from being in the performance-critical path, preventing stalls that waste energy.



The core is also designed to handle memory-intensive workloads more efficiently, as these can burn significant amounts of power in the datacentre. It uses a new split instruction cache comprised of a single-cycle, low-power 24 kB L0 instruction cache complementing its 64 kB L1 I-cache. The two caches are managed exclusively to provide a total of 88 kB of low-latency I-cache. The core also supports a 32 kB L1 Data cache with a 3-cycle load-use latency. This has a multi-level hardware prefetch engine that dynamically adapts to system conditions.

The 48 Falkor CPUs (in 24 cores) are connected by a high bandwidth, low-latency ring interconnect extending out to its large L3 cache and multiple memory controllers, avoiding on-die non-uniform memory access (NUMA) effects (see diagram above).

The chip is in a 55 x 55mm socketed package and is sampling to key customers (think Google, Facebook and Amazon) and will enter production later this year. Qualcomm has also released a motherboard design based around Microsoft's Project Olympus specification that is used by the Open Compute Project Foundation to standardise datacentre building clocks.

Also in the news; No time to ask the Cloud: Qualcomm buys Dutch machine learning start-up

Complete article, here

Embedded FTP server for simple data exchange, in a free PC tool

Segger (Hilden, Germany) has written a free tool that runs in conjunction with its embOS/IP FTP Server add-on. The tool serves as a full FTP Server that is set up with minimal effort. It will run on a Windows, Mac or Linux based machine.

The FTP server tool enables a simple and convenient way to exchange data between any device that can support the FTP protocol as a client and an associated computer. This means that the connected device can transfer acquired data to the computer for analysis purposes or, conversely, access data needed by an operative in order to carry out specific tasks. This includes operations such as transferring media data or presentation from the computer to a tablet. The tool includes an intuitive graphical user interface for quick configuration of the server settings, and login credentials, as well as displaying status information such as connections to the server.

As Segger is a provider of software targeted at resource constrained embedded systems, this PC tool also presents a quick and easy method via which to evaluate the FTP server without requiring any embedded hardware. The PC application behaves exactly as if the server was running on a complete embedded system.

Segger's general purpose FTP server is optimized to provide file sharing via FTP on embedded devices. Typical applications are the uploading of firmware upgrades and bulk file uploads, as well as the downloading of data from storage and media devices. It supports multiple connections and can be used with any file system.

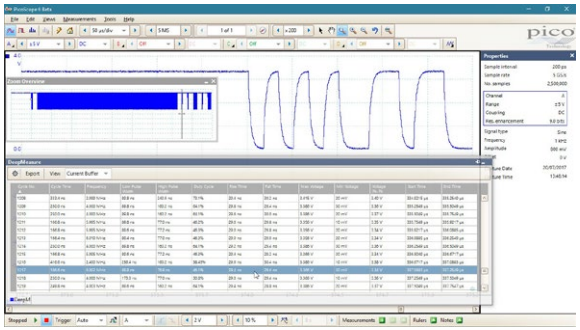
Complete article, here

USB scopes gain automated waveform analysis & tabulation features

Pico Technology, maker of PC oscilloscopes and data loggers, has added the "DeepMeasure" analysis tool to its offering; the waveform analysis and search feature helps to validate the characteristics and performance of complex devices.

Included as standard with PicoScope 3000, 4000, 5000, and 6000 Series oscilloscopes, DeepMeasure delivers automatic measurement of waveform parameters on up to a million successive waveform cycles. Results can be sorted, analyzed and correlated with the waveform display.

Design engineering teams, Pico says, need better tools to record, analyze and visualize waveform data and measurement statistics. Most digital oscilloscopes provide automated measurements of common parameters such as frequency, period, rise and fall times, duty cycle, and maximum and minimum voltages, but the measurements are usually limited to a single complete waveform cycle captured in the oscilloscope memory.



Oscilloscopes with deep capture memory, such as the PicoScope 3000 Series (512 MSamples) and 6000 Series (2 GSamples) can capture waveforms with thousands of waveform cycles, at full sampling speed with each triggered acquisition. DeepMeasure returns a table of results that includes every waveform cycle captured in the memory. Ten waveform parameters are included in the first version of the tool and over a million results of each parameter can be collected.

The table of captured results can be sorted by each parameter in ascending or descending order, enabling engineers to spot anomalies and rapidly identify the cause of complicated issues. So, for example, click on the Rise Time column heading and you can quickly find the fastest (or slowest) rise time out of up to 1 million cycles of the waveform. Double-clicking on a specific measurement highlights the corresponding cycle in the oscilloscope view.

For more extensive analysis, such as histograms and advanced data visualization, the table of measurements can be exported for use with tools such as Excel and MATLAB. More news from the USB-instrument specialist; Modbus decode on Pico USB scope pins down PLC problems

Complete article, here

Automotive Grade Linux speeds in-car infotainment developments

Renesas has started volume shipment of its first R-Car system-on-chip (SoC) incorporating Automotive Grade Linux (AGL)-based software. AGL is a cross-industry effort to develop a fully open software stack for the connected car.

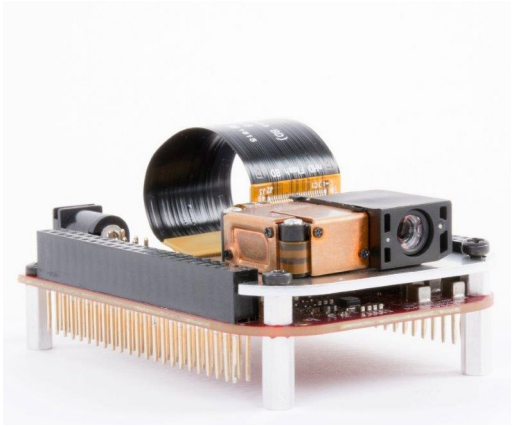
Renesas comments that it considers AGL as an essential step to expand the base of software developers. The Renesas R-Car Starter Kit and AGL-based software is accelerating the development of automotive in-vehicle infotainment (IVI) applications, and moving car makers closer to the realization of connected cars. Renesas is a platinum member of the AGL Collaborative Project, and car makers such as Toyota are participating to promote open source software development. By supporting these activities, Renesas

anticipates it will become possible for more system manufacturers to easily develop automotive applications, even for developers who are not accustomed to embedded application software development, which will contribute to accelerating IVI deployments.
Renesas' first R-Car SoC incorporating AGL platform-based software has started volume shipment for Toyota's new 2018 Camry which is scheduled to come to market in late summer 2017 in the U.S. and will be Toyota's first car model to run Automotive Grade Linux (AGL) software for its infotainment system.
The announcement from the AGL project adds;
The AGL infotainment platform was built from the ground up by hundreds of engineers across the industry who contributed code to develop a robust, Linux-based operating system and application framework with increased security and capabilities. Automakers and suppliers can customize the platform with features, services and branding to meet their product and customer needs. Toyota actively contributes code back to the AGL platform and will be sharing additional code as their next-generation infotainment system is rolled out.
Automotive Grade Linux is a collaborative open source project that is bringing together automakers, suppliers and technology companies to accelerate the development and adoption of a fully open software stack for the connected car. With Linux at its core, AGL is developing an open platform from the ground up that can serve as the de facto industry standard to enable rapid development of new features and technologies. Although initially focused on In-Vehicle-Infotainment (IVI), AGL is the only organization planning to address all software in the vehicle, including instrument cluster, heads up display, telematics, advanced driver assistance systems (ADAS) and autonomous driving. The AGL platform is available to all, and anyone can participate in its development. www.automotivelinux.org/ see also; www.linuxfoundation.org

Complete article, here

TI packages DLP Pico projector display tech for "any low-cost processor"

With a $99 evaluation kit/module, Texas Instruments aims to widen design-ins of its projection-based, ultra-compact display technology.
Developers can, TI says, implement DLP ('digital light processing') display technology with almost any low-cost processor.
The 0.2-inch DLP2000 chipset and $99 DLP LightCrafter Display 2000 evaluation module (EVM) now make it more affordable to make use of DLP technology and design on-demand, free-form display applications such as mobile smart TVs; pico projectors; digital signage; projection displays for smart homes, smartphones and tablets; and control panels and Internet of Things (IoT) display solutions.



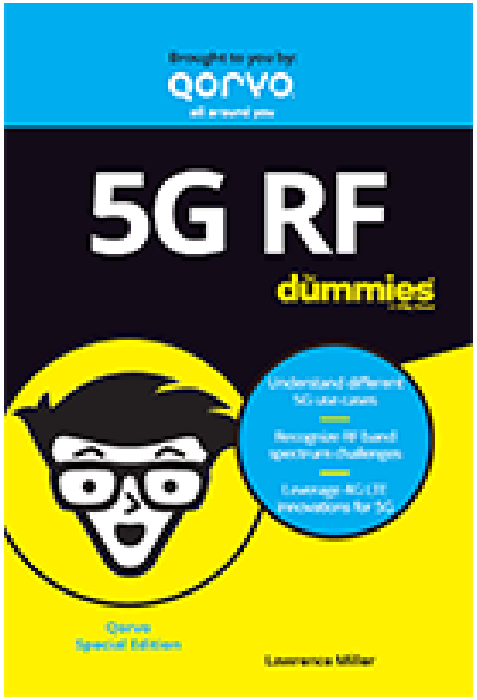
The EVM's dual connector is set up to support any flexible GPIO-driven video interface capable of up to 24-bit RGB-including the BeagleBone Black development board based on TI Sitara AM335x processors, and includes software drivers and BeagleBone Black code examples for easy programming. This makes the technology more accessible for developers to incorporate DLP Pico displays

into new applications.
The 0.2-inch diagonal display is based on the smallest DLP Products digital micro-mirror device (DMD), designed for compact, space-constrained display applications. The EVM features a standard interface and plug-and-play functionality for quick assessment, allowing signals from the display controller to connect with any 24-bit RGB-capable processor and providing solutions with a high-definition (HD) aspect ratio.
The DLP2000 is available now for $19.99 and the DLP LightCrafter Display 2000 EVM is available for $99.00 through the TI store and authorized distributors.

Complete article, here

"5G RF For Dummies" E-Book

RF-silicon-maker Qorvo has written and published a book on RF considerations for 5G communications, under the familiar "...for Dummies" logo. This one, Qorvo says, will help, "Get ready for the future of IoT and mobile communication."
"5G RF For Dummies" aims to to help you learn how innovations such as carrier aggregation (CA), massive multiple input/multiple output (MIMO), and densification of small cells are ushering in the 5G era.
Written in conjunction with publisher John Wiley and Sons, Inc., the free, 44-page booklet provides an in-depth look at 5G – considered the future of the Internet of Things (IoT) and mobile communications.
5G RF For Dummies helps technical and nontechnical professionals understand how 5G will evolve and connect the world around us. The e-book also offers unique



insight into 5G trends, use cases, roadmaps, the key role RF technology plays, and how 4G LTE is the building block to implementing 5G.
Qorvo's experts address many important aspects of 5G from both the mobile and infrastructure perspectives.
The text provides an overview of issues such as;
- Which visions and trends are driving us to a 5G future
- How 5G technology will cohesively connect many industries in a diverse and flexible way
- How 5G will use and reshape the frequency spectrum more efficiently than current technologies
- Which RF communications technologies are enabling the use cases and path to 5G
- Important milestones to look for in the development of 5G

Complete article, here

Cypress smart home platform gets an ear for Siri by Christoph Hammerschmidt

With the latest release of its IoT development platform WICED (Wireless Internet Connectivity for Embedded Devices) Studio, Cypress Semiconductor makes it easier to enable Smart Home applications to communicate wirelessly: The platform now

supports Apple's HomeKit toolbox. The support also extends to Apple's voice control technology Siri.

Using Cypress' WICED development platform and ultra-low power CYW20719 Bluetooth/BLE MCU, developers can integrate HomeKit support into products such as smart lighting devices, leverage Siri voice control and connect to the Apple Home app seamlessly. WICED Studio provides a single development environment for multiple wireless technologies, including Cypress' s Wi-Fi, Bluetooth and combo solutions, with an application programming interface in the wireless SDK.

The Cypress CYW43907 SoC integrates dual-band IEEE 802.11b/g/n Wi-Fi with a 320-MHz ARM Cortex-R4 RISC processor and 2 MB of SRAM to run applications and manage IoT protocols. The SoC's power management unit simplifies power topologies and optimizing energy consumption. The WICED SDK provides code examples, tools and development support for the CYW43907.

The WICED platform supports a broad range of other popular cloud services and eliminates the need for developers to implement the various protocols to connect to them, reducing development time and costs. The WICED Studio SDK enables cloud connectivity in minutes with its robust libraries that uniquely integrate popular cloud services such as iCloud, Amazon Web Services, IBM Bluemix, Alibaba Cloud, and Microsoft Azure, along with services from private cloud partners and China's Weibo social media platform.

In line with the IoT trend toward dual-mode connectivity, the kit supports Cypress' Wi-Fi and Bluetooth combination solutions and its low-power Bluetooth and Bluetooth Low Energy (BLE) combination solutions.

Complete article, here

Secure Cortex-M4F MCU integrates contactless interface and XiP Quad SPI

Maxim Integrated has posted outline details of its MAX32566 DeepCover secure microcontroller, configured as a secure and cost-effective solution for new generations of trusted devices for mobile payment. It includes an RF contactless radio for fast, reliable communication.

The SoC is based around a low-power, ARM Cortex-M4 (with floating point unit) and is equipped with Maxim's DeepCover embedded security solutions to cloak sensitive data under multiple layers of advanced physical security to provide the most secure software protection possible.

The ARM Cortex-M4 with FPU core supports a 96 MHz system clock. Multiple power operating modes and dynamic clock gating minimize power consumption while maintaining high-performance on demand. Up to 128 MB of external, encryptable flash memory is supported on a high-speed SPI bus, allowing for XiP (execute-in-place) operation. Portions of the internal 128 kB SRAM are encryptable and can be battery-backed for secure and reliable storage.

Multiple security features create a secure cryptographic boundary that protects program code and data. Environmental, microprobe, and user-configurable external dynamic tamper sensors can trigger a system-level tamper response, erasing secret keys and rendering internal and external memory unreadable. A secure keyboard controller provides a user interface while protecting against unauthorized access. High-speed cryptographic accelerators and a random number generator support highly secure communications.

Complete article, here

Mesh networking capability added to Bluetooth

In July, the Bluetooth Special Interest Group (SIG) announced that Bluetooth technology now supports mesh networking. The new mesh capability enables many-to-many (m:m) device communications and is optimized for creating large-scale device networks. The announcement was immediately followed by silicon vendors (examples, below) in the sector with their own disclosures of stack updates to accommodate mesh.

The extension of Bluetooth is a software/firmware update and is implemented within the Bluetooth protocol stack; no physical-level changes are involved and Bluetooth Mesh will run on Bluetooth Low Energy (LE) hardware and silicon.

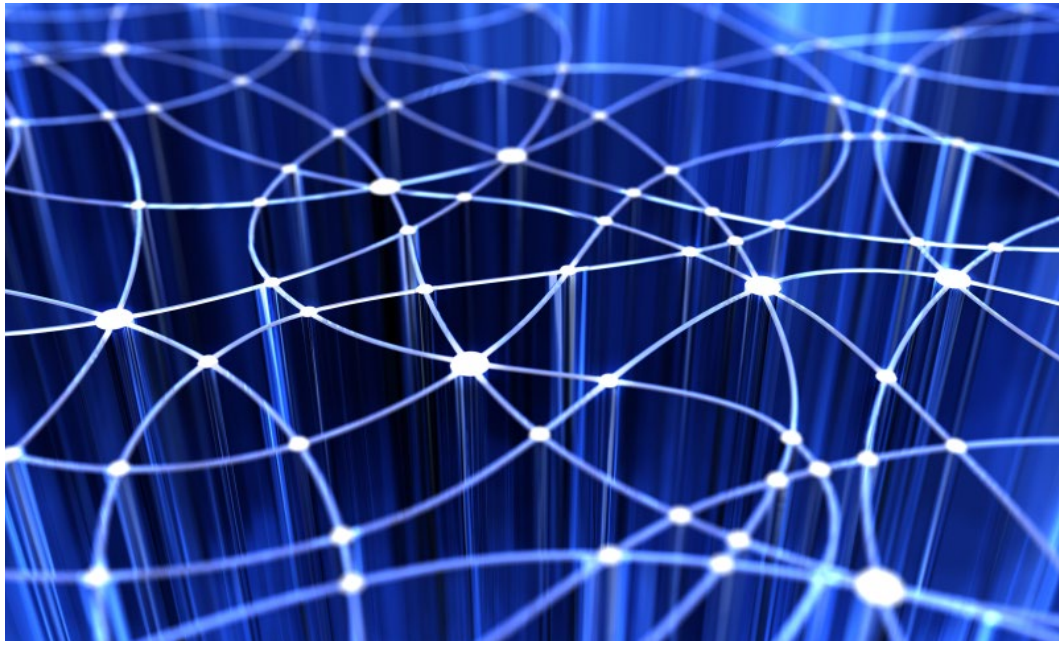
The SIG says that Bluetooth mesh is suited for building automation, sensor networks and other IoT solutions where tens, hundreds, or thousands of devices need to reliably and securely communicate with one another.

Commercial building and factory automation, the SIG adds, represent major market opportunities for wireless mesh networking technologies. These markets demand true industrial-grade solutions, which Bluetooth mesh uniquely delivers, with features including;

- Reliability: Enables inherently self-healing networks with no single points of failure
- Scalability: Supports thousands of nodes with industrial-level performance
- Security: Provides industrial-grade security for protection against all known attacks

The SIG proposes the appeal of Bluetooth mesh to be that it delivers proven, global interoperability that assures products from different vendors work together, with attributes quoted as;

- Full-stack solution: A unique full-stack approach defines the low-level radio up to the high-level application layer, ensuring all aspects of the technology are fully specified
- Interop-centric specification: Comprehensive, multi-vendor interoperability testing is conducted during the specification development process, not after specification release
- Time-tested tools and processes: A 20-year history of delivering the qualification tools and processes needed to ensure global, multi-vendor interoperability



A mesh network built using Bluetooth technology can, the SIG concludes, support additional services, such as asset tracking and way finding; and it comes with a known branding.

The Bluetooth mesh networking specifications, as well as the tools required to qualify Bluetooth products with mesh networking support, are now available at the Bluetooth website. Bluetooth mesh networking operates on Bluetooth Low Energy (LE) and is compatible with core specification version 4.0 and higher.

One of the silicon vendors poised to announce product at the same time as the Bluetooth SIG's disclosure of mesh operation is Silicon Labs, which says that its offering will help developers cut time to market by as much as six months. Silicon Labs has introduced a suite of software and hardware that supports the Bluetooth mesh specification that includes development tools, a software stack, and mobile apps for smartphones supporting Silicon Labs' wireless system-on-chip (SoC) devices and certified modules. The software update runs on top of Bluetooth 4.0, and so is compatible with all existing BLE hardware; similarly the smartphone app "doesn't touch" native Android or IoS functionality.

Silabs expects to see Bluetooth mesh devices first in lighting, both commercial and domestic; and in smart home applications, and in beaconing and asset tracking. A mesh network enables devices, such as connected lights, to be deployed at greater distances from a hub or gateway. By combining Bluetooth LE with mesh networking, new capabilities and value can be introduced into devices such as connected lights which can also serve as beacons or beacon scanners.

Silicon Labs; www.silabs.com/bluetooth-mesh

Nordic Semiconductor also added Bluetooth mesh support with nRF5 SDK for Mesh; this Software Development Kit enables developers to embark on Bluetooth mesh designs with Nordic's nRF51 and nRF52 Series SoCs immediately upon official stack adoption by Bluetooth SIG. The ultra low power (ULP) RF specialist synchronised its introduction of "nRF5 SDK for Mesh" with the disclosure of the mesh operating mode by the Bluetooth SIG.

nRF5 SDK for Mesh can be downloaded from Nordic's website and includes the company's first release of its Bluetooth mesh software protocol ("stack"). The SDK is compatible with the nRF51 and nRF52 Series Systems-on-Chip (SOCs), and the S110, S130, and S132 Bluetooth 4.0-compatible SoftDevices (Nordic's Bluetooth low energy stacks). With the nRF5 SDK for Mesh, developers who already have a Nordic nRF52 Development Kit (DK) can immediately start building Bluetooth mesh-based applications.

Nordic's Bluetooth mesh stack incorporates additional features not included in the Bluetooth SIG's Bluetooth mesh 1.0 specification. Nordic's stack includes secure side-by-side and blocking device firmware updates (DFU), a feature which allows scalable, secure DFU across the mesh without interruption of service while the new firmware is transferred.

The Nordic Bluetooth mesh stack also includes a solution for provisioning over relaying nodes and a serialization interface which allows control of the mesh over a serial interface when using a two-chip Bluetooth mesh solution.

The alpha version of the nRF5 SDK for Mesh is available from www.nordicsemi.com

Toshiba Electronics Europe likewise announced that its Bluetooth Low Energy products now offers support for the Bluetooth Mesh standard. By combining a non-proprietary mesh solution with Toshiba Bluetooth communication system solutions (which are capable of link budgets exceeding 100 dB with external PA and LNA), Toshiba extends its BLE technology to provide more reliable communication in consumer products and extend new support to rapidly growing segments such as factory automation and building management.

Support for the new Bluetooth Mesh standard 1.0 now enables Toshiba Bluetooth Low Energy products to privately and securely relay messages via a mesh network rather than requiring a point-to-point connection between devices. This increases the range and reliability of Bluetooth Low Energy communication without increasing power requirements.

https://toshiba.semicon-storage.com/eu/product/wireless-communication/bluetooth.html

Complete article, here

MAXIMIZE RUN TIME IN AUTOMOTIVE BATTERY STACKS, AS CELLS AGE

By Samuel Nork and Tony Armstrong, Linear Technology

Large battery stacks consisting of series-connected, high energy density, high peak power lithium polymer or lithium-iron phosphate ($LiFePO_4$) cells are commonplace in applications ranging from all-electric (EV or BEV) and hybrid electric vehicles (HEVs and plug-in hybrid electric vehicles or PHEVs) to energy storage systems (ESS).

The electric vehicle market in particular is forecast to create tremendous demand for large arrays of series/parallel connected battery cells. The 2016 global PHEV sales were 775,000 units [Source: EVvolumes.com], with a forecast of 1,130,000 units for 2017. Despite the growing demand for high capacity cells, battery prices have remained quite high and represent the highest priced component in an EV or PHEV with prices typically in the $10,000 range for batteries capable of a few hundreds of kilometres of driving range. The high cost may be mitigated by the use of low cost/refurbished cells, but such cells will also have a greater capacity mismatch, which in turn reduces the usable run time, or drivable distance on a single charge. Even the higher cost, higher quality cells will age and develop mismatch with repeated use. Increasing stack capacity with mismatched cells can be done in two ways: either by starting with bigger batteries, which is not very cost effective, or by using active balancing, a technique to recover battery capacity in the pack which is quickly gaining momentum.

All series-connected cells need to be balanced

The cells in a battery stack are balanced when every cell in the stack possesses the same state of charge (SoC). SoC refers to the instantaneous value of the remaining capacity of an individual cell relative to its maximum capacity, as the cell charges and discharges. For example, a 10A-hr cell with 5A-hrs of remaining capacity has a 50% SoC. All battery cells must be kept within a SoC range to avoid damage or lifetime degradation. The allowable SoC min and max levels vary from application to application. In applications where battery run time is of primary importance, all cells may operate between a min SoC of 20% and a max of 100% (or a fully charged state). Applications that demand the longest battery lifetime may constrain the SoC range from 30% min to 70% max. These are typical SoC limits found in electric vehicles and grid storage systems, which utilize very large and expensive batteries with an extremely high replacement cost. The primary role of the battery management system (BMS) is to carefully monitor all cells in the stack and ensure that none of the cells is charged or discharged beyond the min and max SoC limits of the application.

With a series/parallel array of cells, it is generally safe to assume the cells connected in parallel will auto-balance with respect to each other. That is, over time, the state of charge will automatically equalize between parallel connected cells as long as a conducting path exists between the cell terminals. It is also safe to assume that the state of charge for cells connected in series will tend to diverge over time due to a number of factors. Gradual SoC changes may occur due to temperature gradients throughout the pack or differences in impedance, self-discharge rates or cell-to-cell loading. Although the battery pack charging and discharging currents tend to dwarf these cell-to-cell variations, the accumulated mismatch will grow uchecked unless the cells are periodically balanced. Compensating for gradual changes in SoC from cell to cell is the most basic reason for balancing series-connected batteries. Typically, a passive or dissipative balancing scheme is adequate to re-balance SoC in a stack of cells with closely matched capacities.

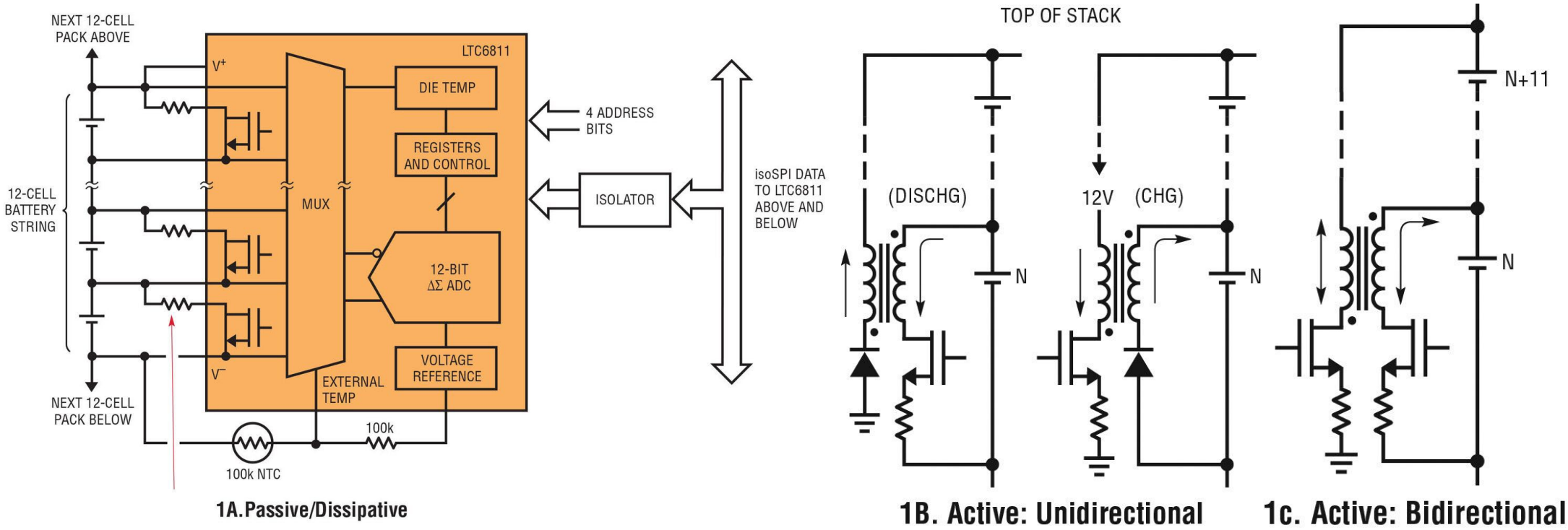


Figure 1. *Typical cell balancing topologies*

As illustrated in Figure 1a, passive balancing is simple and inexpensive. However, passive balancing is also very slow, generates unwanted heat inside the battery pack and balances by reducing the remaining capacity in all cells to match the lowest SoC cell in the stack. Passive balancing also lacks the ability to effectively address SoC errors arising from another common occurrence; capacity mismatch. All cells lose capacity as they age and they tend to do so at different rates for reasons similar to those listed above. Since the stack current flows into and out of all series cells equally, the usable capacity of the stack is determined by the lowest capacity cell in the stack. Only active balancing methods such as those shown in Figures 1b and 1c can redistribute charge throughout the stack and compensate for lost capacity due to mismatch from cell to cell.

The continuation of this article describes the implementation of an active cell-to-cell charge balancing scheme; click the panel below for full pdf.

A DUAL-CHANNEL ADC… OR IS IT A QUAD?

BY UMESH JAYAMOHAN, ANALOG DEVICES

Ever since the advent of the very first monolithic, silicon-based analogue-to-digital converters (ADCs), the ADC has been keeping pace with the rapid advances in silicon processing technology. Over the years, the silicon processing technology has advanced enough that it is now possible to economically design ADCs with a lot more powerful digital processing. Earlier generation ADC designs used very little digital circuitry outside of error correction and digital drivers. The new family of GSPS (gigasample per second) converters (also known as RF sampling ADCs) are built with sophisticated 65 nm CMOS technology and can pack a lot more digital processing power to enhance the ADC's performance.

With high sample rates (in the GSPS realm) also comes a huge payload of data (bits per second). Take the AD9680, which is a dual 14-bit, 1.25 GSPS/1 GSPS/820 MSPS/500 MSPS, JESD204B analogue-to-digital converter as an example. At the maximum sample rate of 1.25 GSPS, the ADC streams;

14 [bits] × 2 [converter channels] × 1.25 Gbps = 35 Gbps

This amount of data would require an enormous number of LVDS routing lanes to extract the digital data. In order to facilitate the implementation of large throughput, the JESD204B standard was adopted. The JESD204B is a high speed, data transmission protocol that employs 8b/10b encoding and scrambling, among other features, aimed at providing adequate signal integrity. With the JESD204B standard, the total throughput now becomes;

16 [bits] × 2 [converter channels] × (10/8) × 1.25 Gbps = 50 Gbps

Using the JESD204B standard, the data throughput can be split across four high speed serial lanes at 12.5 Gpbs on each lane. Compare this to an LVDS interface where, at a line rate cap of about 1 Gbps/lane, the chip would need more than 28 pairs!

A quick inspection of the AD9680 data sheet reveals that there is a real "alphabet soup" as far as setting up the link goes. Whereas earlier generation LVDS ADCs were easier to implement, the newer generation JESD204B ADCs are a bit more complicated. They become even more complicated when you take into account the internal digital downconverter (DDC) setups. However, the ADC setup is primarily determined by three letters in that alphabet soup:

L = number of lanes per JESD204B link
M = number of converters per JESD204B link
F = number of octets per frame of data in the JESD204B link

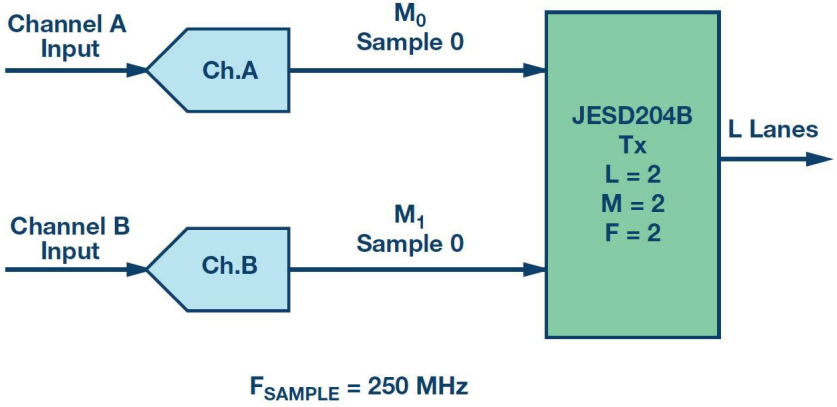


Figure 1. *Setting up the AD9250.*

Take for example the AD9250, which is a dual 14-bit, 250 MSPS JESD204B analogue-to-digital converter. Figure 1 shows the block diagram representation of the AD9250 in its default setup.

In this setup the JESD204B link (JESD204B transmitter) is pretty straightforward, as there is no additional digital processing done in the AD9250. To the JESD204B link, Channel A becomes Converter 0 (M0), whereas Channel B becomes Converter 1 (M1), which means the value of M becomes 2. The total line rate for this setup is;

Line Rate = (M × N' × (10/8)× F_{OUT}) / L =

(2 × 16 × 1.25 × 250M) / 2 = 5 Gbps/lane

Compare this to the AD9680 sampling at 1 GSPS—but in this case, two digital downconverters are used in a complex (I/Q) setup. Figure 2 shows the AD9680 where the digital downconverters are used to decimate the data sampled at 1 GSPS by four. This results in an output sample rate (F_{OUT}) of 250 MSPS.

It is clear from Figure 2 that the AD9680 can effectively reduce the sample rate using the internal on-chip digital downconverters. Since each of the DDCs outputs a 16-bit stream, the actual (physical) converter bit streams are now decoupled from the "M" parameter of the JESD204B alphabet soup. Per the standard, M is the number of converters per link. In the modified scenario, M now becomes a parameter called a virtual converter. Even though the AD9680 physically only has two ADC channels (A and B), with the DDCs in complex output mode enabled, there are now four different (16-bit) data streams to the JESD204B interface. To the JESD204B interface, this looks like there are now four (virtual) converters sending bit streams. Hence, the M = 4 or "converter multiplying act". The output line rate in this case becomes;

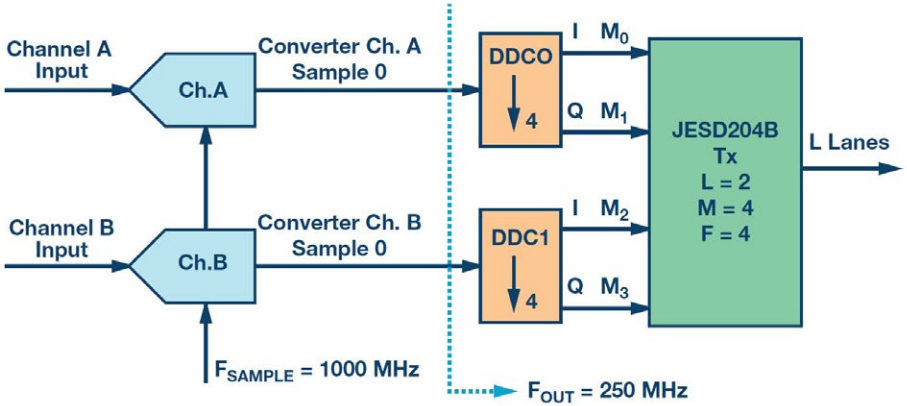


Figure 2. *Setting up the AD9860-1000 with two DDCs set to decimate by 4.*

Line Rate = (M × N' × (10/8)× F_{OUT}) / L =

(4 × 16 × 1.25 × 250M) / 2 = 10 Gbps/lane

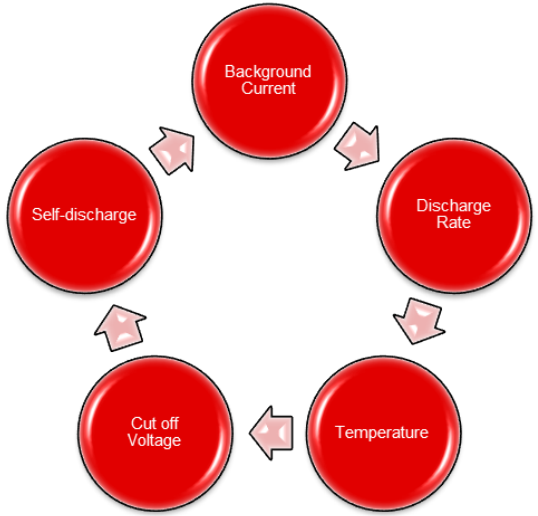
The flexibility of the AD9680's JESD204B interface becomes apparent here, as there are now two options available depending on what the line rate acceptability of the receive logic (ASIC or FPGA). Table 1 and Table 2 (click this link to download) show, respectively, the available options for the JESD204B interface in the AD9680 setup shown in Figure 2, and, for a dual-channel ADC like the AD9680 that has four DDCs, the virtual converter mapping that is available for various configurations.

Umesh Jayamohan *[umesh.jayamohan@analog.com] is an applications engineer with Analog Devices in the High Speed Converter Group (Greensboro, NC). He has been a part of Analog Devices since 2010. Umesh received his B.S.E.E. from the University of Kerala, India, in 1998, and his M.S.E.E. from Arizona State University in 2002.*

SMARTER POWER FOR THE FRONT-END OF THE INTERNET OF THINGS

Eric Djakam, Texas Instruments

The Internet of Things, or so called “next industrial revolution” is changing the way all businesses interact with the world. Sensor technologies are at the heart of the IoT and most of these sensors are expected to be powered using primary battery sources, mainly due to the fact that many of the applications such as smart parking controls or smart metere, require the product to be sealed. These products are expected to operate in the field without any modification to the hardware for their life-time.



Any malfunctions of the system, either of hardware or software will impact its life time on the field and should be quickly addressed before the battery is depleted. This article describes an approach to achieving that objective.

Accurately monitoring lithium thionyl chloride (Li-$SOCl_2$) and lithium manganese dioxide (Li-MnO_2) batteries - that is, lithium-based primary batteries - is challenging. A purpose-designed monitoring IC simplifies this task and allows the designer to focus on other functions of the end-product. The device is used here to demonstrate a technique to implement primary battery monitoring function for IoT applications, taking as an example a smart water meter.

The bq35100 is a fuel gauge designed to accurately monitor Li-$SOCl_2$ and Li-MnO_2 batteries. It uses voltage, current and temperature measurements to calculate other battery parameters:

- State of Charge: The amount of energy remaining in the battery is provided, and can be correlated with the system power consumption to accurately schedule the service replacement.
- Health: Several flags are available, and are based on parameters such as low voltage, low/high temperature, low/high current, low state of charge, and detection of battery removal. They can be used by the network to anticipate issues with battery operating conditions.
- Life time data: It collects the battery in-service data -including min/max cell voltages, min/max discharge current, min/max temperature, which can be used for maintenance purposes when the product reaches the end of its life cycle. For example, such information can help to optimize the software running in the microcontroller by correlating the operating modes with voltage, current and temperature conditions.
- Accumulated capacity: this corresponds with the amount of energy consumed by the system. For example, this parameter can be used to monitor the end equipment’s health. Issues such as short circuits (due to power supplies inductor damage) or malfunctioning of some semiconductor IC or software code could lead to high current consumption, and thereby require unanticipated maintenance of the equipment.

SMART METER SYSTEM REQUIREMENTS

In recent years, utilities have been moving from mechanical to fully electronic meters. We have seen added functionalities such as metrology with ultrasonic technology, leak detection with audio patterns, communication with low power and long range radio, meter anti-tampering detection with, for example, inductive sensing technology, and others, being added to the e-meter. These new functionalities allow utilities to deliver new services such as

POWERING SMART METERS

condition-based maintenance and remote monitoring of meters, which leads to efficient management of the network and better customer experience. As nothing is free, this adds complexity in the power management stages and batteries. On top of this, smart meters are required to operate:
- over a long life time. The typical life time of a smart meter is about 20 years, without modification of the hardware.
- with high dynamic load. As an example, a high power RF amplifier used for the 169 MHz wireless M-bus link is specified to deliver 27 dBm (~500 mW). This represents about 180 mA under 2.8V supply (without taking into account the power supply efficiency). The same system consumes about 5 µA in sleep-mode mode with the metrology front end active. The power management front end should therefore be able handle this dynamic load profile ratio of 36000.

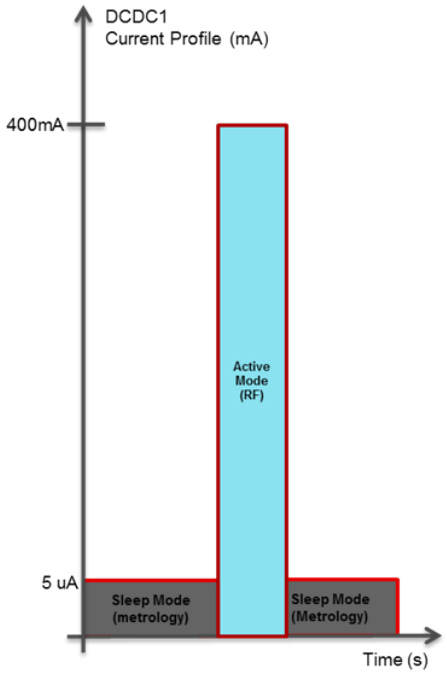


Figure 1. *Typical water meter load profile*

- *with low stand-by power consumption.* The stand-by power consumption of a typical meter is in the range of 5 µA. This is required to guarantee the long life-time of the system.
- *over wide temperature ranges.* Depending on the country, smart meters can be located outside the building in areas subject to high temperature changes. As we will see below, such temperature changes impact the battery performance.
- *with high duty cycle on the current.* The smart meter peak current is usually driven by the communication front end. This function is active once or twice a day to remotely provide the network with end user's data.

A typical smart meter system comprises;
- A metrology front end, which is used to measure the energy consumed by the end user. We have seen inductive, ultrasonic or magnetic technologies being used to implement this function.
- A communication front end is used to feed data to the network. Radio communications are mainly used, with support of different protocols such as Wireless M-Bus (France, Italy), Zigbee (UK), proprietary networks or some new protocols such as Narrowband LTE –Long Term Evolution-, Sigfox or LoRa. Sometimes, local links such as NFC (near field communications) are added on pay as-you-go meters for secured and low range communication.
- The application microcontroller
- A power management block delivers power needed by the different functions. For water and gas meters, the energy sources mainly come from lithium primary batteries.
- A potection front end protects the meter against tampering, by either magnetic or cover-open means.

On the top of those requirements, water and gas meters usually come in small form factors which combined with the presence of RF technologies require very specific system care, at an early stage of the design, to prevent interaction between the different domains (power, metrology, communication).

This article continues by examining the specific characteristics of lithium primary batteries as they affect IoT designs, and outlines principles to optimise product designs. Click the panel below for full pdf.

SIMULATION-DERIVED FIT RATES IMPROVE FAILURE ANALYSIS ACCURACY

Viktor Preis, Frederico Ferlini & Robert Schweiger, Cadence

This article explains a new holistic methodology that combines analytic methodologies such as Failure Modes Effects and Diagnostics Analysis (FMEDA) with fault injection methodologies to significantly increase the confidence of safety analysis data and achieve faster product compliance – especially as it relates to systems that will operate within autonomous vehicles.

Automated fault injection is a well-established test method used to verify the correct implementation of safety mechanisms and to get much more realistic and lower FIT (failure in time) rates than the worst-case values provided by estimations.

The automotive industry is devoting massive resources to developing autonomous cars with two major goals in mind:
- To enable fully automated driving (a completely driverless car)
- To reduce car accidents by making safer vehicles

Advanced driver assistance systems (ADAS) make use of various sensors such as cameras, LIDAR (Light Detection and Ranging), radar and ultrasound to fully sense the environment around the car. These sensors generate a very large amount of real-time data. High-speed communication-based Automotive Ethernet provides the bandwidth to further distribute the data within the car.

In addition to sensors, high-definition digital maps, high-precision positioning, cloud-based services, and vehicle-to-vehicle and vehicle-to-infrastructure (V2X) communication are needed to ensure the robustness, reliability and safety of self-driving cars. As a result, the electronic content of cars is increasing rapidly, relying on a new class of high-performance systems-on-chip (SoCs) to process all sensor data for the control of the vehicle in real time.

A dedicated functional safety verification process for these safety-critical SoCs is needed to achieve the required safety requirements (e.g. ASIL level related design process and FIT rates). ISO 26262 [1] is an accepted standard used to ensure the functional safety (FS) in automotive systems. An extension of the ISO 26262 standard, Edition 2 (set to be published in 2018), will be specifically dedicated to address semiconductor-related failure analysis.

This article describes some important aspects of SoC or IP related functional safety analysis and verification; and continues by introducing some failure modes and safety mechanisms with a concrete example, which was used to introduce the functional safety flow. It continues by describing some main aspects of the functional safety verification flow, and summarises the main achievements.

ASPECTS OF FUNCTIONAL SAFETY ANALYSIS AND FUNCTIONAL SAFETY VERIFICATION

All safety-critical subsystems contribute to the overall safety of the car. Therefore, a comprehensive safety architecture is key to achieve required safety goals. As subsystems contain more and more SoCs, the safety features of the SoCs are a critical part of the complete safety of subsystems and at the end of the car. Hence, it's also important that safety features of the IP (Intellectual Property) blocks, which make up the subparts of a SoC, can be leveraged at SoC level, reducing overall safety compliance effort.

FUNCTIONAL SAFETY ASPECTS OF SOCS

Today's high-performance SoCs consist of hundreds of functions implemented in IP blocks, comprising many millions of transistors. Together with the high density of the technology nodes this results in a high

FIT rate. FIT rates greater than 100 FIT for single SoC are common [2]. The ISO 26262 standard requires the probabilistic metrics for random hardware failures of less than 100 FIT for ASIL-B and ASIL-C and less than 10 FIT for ASIL-D items. Moreover, very conservative estimation starts with several hundreds of SoCs within a single car. Therefore, FIT rate reduction methods are crucial for using SoCs in safety-critical systems.

SOC FIT RATE REDUCTION METHODS

There are basically two methods to reduce the FIT rate of an SoC to achieve the given functional safety requirements.

The first method is based on the fact, that out of the hundreds of functions of an SoC not all are related to the safety requirements of the system. The idea is: reduce the FIT rate of an SoC to the portion which is critical for the safety requirement. This reduction is done using systematic approaches for qualitative and quantitative analysis.

However, this approach is not sufficient and hence leads to the second, supportive method, namely adding safety mechanisms to the design. Without safety mechanisms it is basically impractical to achieve the mandatory risk reduction for SoCs.

The main goal of a safety mechanism is to detect faults and to initiate appropriate measures, e.g., to get the system in a safe state (fail safe requirements) or even to correct faults to continue normal operation (fail operational requirements).

Safety mechanisms can be very efficient in detection of more than 99% of related faults. But they represent additional cost in terms of chip area, power and possible performance loss. The cost is even higher if the safety mechanisms are targeted to correct the errors. A thorough analysis of required safety mechanism capabilities and safety mechanism architecture is mandatory.

FUNCTIONAL SAFETY ANALYSIS

The ISO 26262 standard recommends various methods for functional safety analysis. One of the commonly used methods for qualitative analysis is Failure Mode Effect Analysis (FMEA). The primary goal of an FMEA is to understand the impact of potential failures and to specify a functional safety architecture of safety mechanisms to handle the failures.

Failure Mode Effect and Diagnostic Analysis (FMEDA) determines the diagnostic coverage (DC) for residual and latent faults. These values together with the FIT rate refinement of the FMEDA result in the hardware architectural metrics calculation, e.g. Single Point Fault Metric (SPFM) and Latent Fault Metric (LFM). The hardware architecture metrics (SPFM, LFM) reveal whether the diagnostic coverage of a safety mechanism is sufficient (ISO 26262 refers).

Starting from an FMEDA, the safety designer usually allocates the FIT rates for the SoC and all sub-components. The design related data (e.g. number of transistors) is provided by the fault injection technology, as fault injection technology has access to design related information. A further refinement splits the SoC level failure modes into failure modes of the sub-components. Using the design data of the fault injection technology, the distribution of these failure modes is calculated.

FUNCTIONAL SAFETY VERIFICATION

The functional safety analysis can be done based on estimated values for diagnostic coverage of the safety mechanisms. This is a common way for initial analysis run before any design exists. It is also often used for smaller SoCs targeted to maximise ASIL-B. Often this method is used due to lack of effective tool support e.g. fault injection technology. However, fault injection is mandatory when executing functional safety verification targeting ASIL-C and ASIL-D.

Estimated values for diagnostic coverage of safety mechanisms inherit several weaknesses which have effect on the results:
- Estimation is performed coarse-grained. To increase confidence during analysis, worst-case values (resulting in higher FIT rates) are taken as estimated values. Hence, the estimated values can be too conservative.
- Additionally, there is a gap between estimated values for a safety mechanism and the real, implemented safety mechanism design. Diagnostic coverage estimations are always related purely to the safety mechanism function. They do not take the surrounding system into account.
- There is no support for estimation of latent faults, except to select a very conservative value.

Fault injection technology bridges the gap between the conservative estimated and the more realistic design related values. It represents a much more reliable way to prove much better diagnostic coverage results.

Functional safety verification at FMEA level allows proof of the correctness of the failure impact analysis and proof of the correctness of the functional safety architecture. At FMEDA level, functional safety verification allows proof of the effectiveness of the implemented safety mechanism architecture and permits calculation of more accurate and less conservative hardware architectural metrics.

FAULT CLASSIFICATION

A targeted fault injection flow allows simulation of the influence of a fault on the failure modes, i.e. whether a fault propagates to the failure mode and hence violates the system function. As a result of fault injection, the fault can be classified. These fault classifications are required for the hardware architectural metrics calculation.

Faults can be classified in several categories based on the annotated result from fault injection flow. Out of the fault classifications defined by the ISO 26262 standard the following are of main interest for SoC analysis:
- *Safe faults:* faults that cannot propagate into the system and have no impact on the correct operation of the system;
- *Detected faults:* faults which propagate to the system, and hence potentially violate the systems correct operation, but are detected by safety mechanisms;
- *Residual faults:* faults which propagate to the system, and hence potentially violate the systems correct operation, and which are not detected;

- *Latent faults:* faults which on their own do not propagate into the system, i.e. do not violate the correct functionality, but together with another fault may violate the system.

This article continues with an examination of the specific case of verifying safe operation in Ip for an automotive Ethernet node; and reports experimental comparisons of methods of verifying safe operation. Click panel below for full pdf.

Download PDF of Article

Find Automotive SOC Safety on EETsearch

EIGHT STEPS TO BETTER ADAS SOFTWARE

Dr. Alexander Hertz, Tasking, & Mark Forbes, Altium

Developing ADAS software can be challenging and time consuming. Safety is of paramount concern, with reliability at the same level. In this article, we aim to show eight steps that can not only shorten design time, but help with safety and reliability as well. We will use a multicore processor as an example as multicore technology is very popular in automotive applications.

STEP 1: DRIVER AND RTOS SUPPORT

After choosing a specific device for a project, you need to select a compiler toolchain vendor and version that is compatible with the drivers, libraries, and RTOS versions for your target device. These typically include MCAL for AUTomotive Open System ARchitecture (AUTOSAR), SafeTLib and Secure Hardware Extension (SHE) for safety applications, and potentially additional libraries for, for example, encryption, and linear algebra manipulations.

The MCAL requires some careful thought about dependencies, as shown in Figure 1. In general, the target device vendor and RTOS vendor offer support for the compiler version of your choice. However, certification of all the necessary drivers and configuration files requires significant effort and time. In time-constrained situations, it may make sense to choose a combination of drivers and compiler version that is available off the shelf.

Cross linking enables you to safely mix binaries (such as MCAL drivers) created with older compiler versions with binaries of code compiled using current versions. Reusing old code and binaries can save time and money, while using the latest compiler optimizations for new applications can improve performance – allowing your application to fit into a smaller, cheaper device.

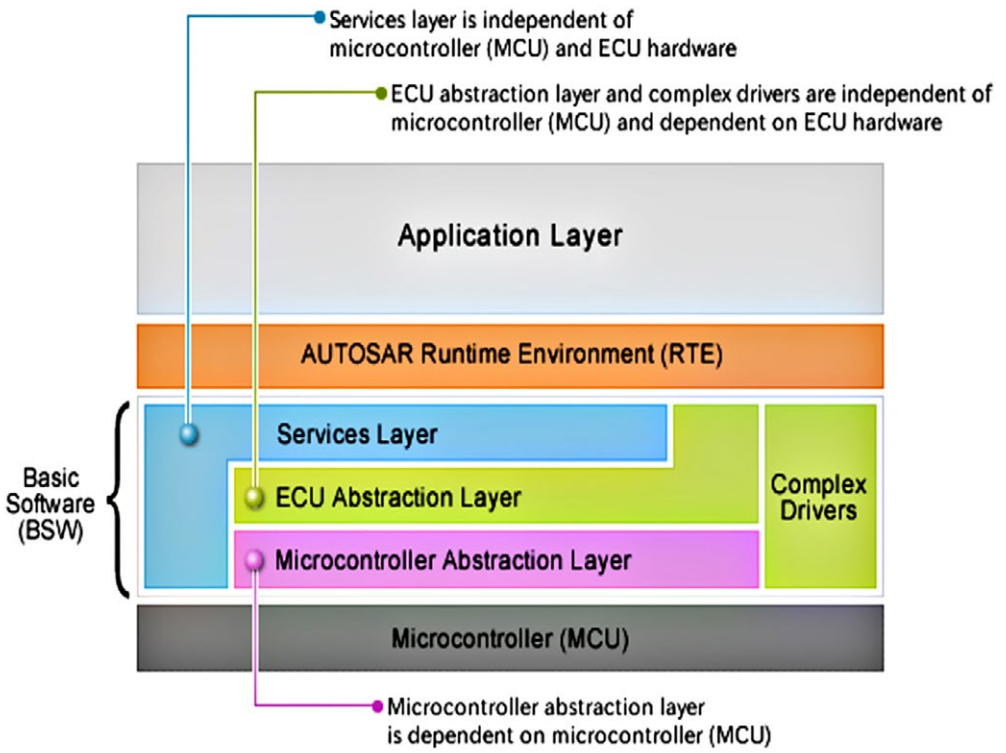


Figure 1. *The MCAL is dependent on the MCU selected.*

In addition to compiling the MCAL drivers with an older compiler release, any pre-certified older code can be reused unchanged. Current applications and new code that is not bound to an old compiler version can instantly benefit from performance gains and improvements available with the latest compiler technology.

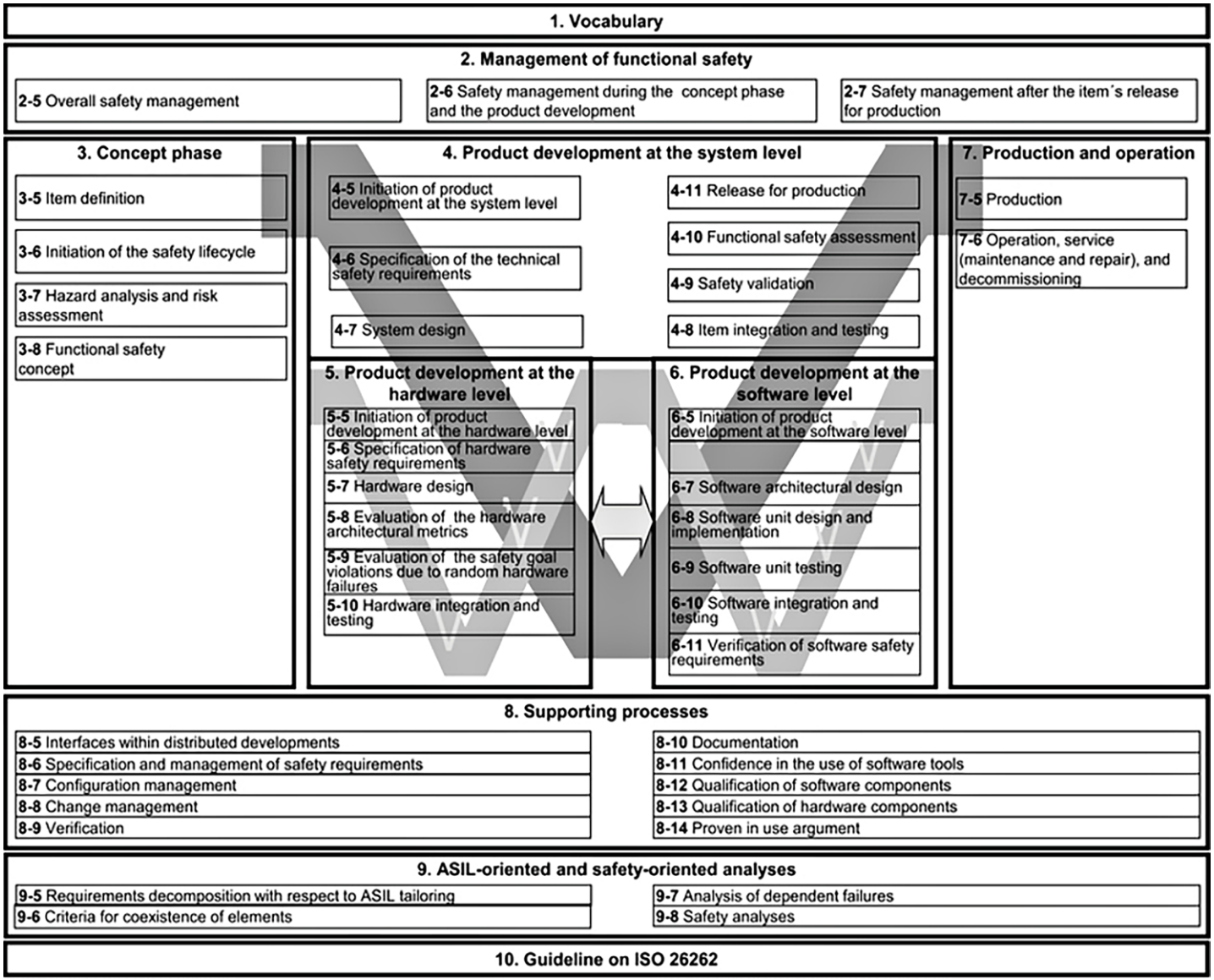


Figure 2. *Guidelines for ISO 26262*

STEP 2: SAFETY AND PERFORMANCE

Safety and performance of tools and their output are often handled as separate, discrete topics. Some developers may benchmark different compiler vendors to find the best tool for an application, then separately evaluate safety feature information. However, what is the value of having the best benchmarks if you must turn off many of the best features and optimizations because they may fail in corner cases?

Safety; ISO 26262-6 specifies guidelines for automotive product development at the software level (see Figure 2). To comply with these guidelines, you must choose software development tools that are safety certified. Important considerations when selecting a software toolset include:

- Developed per ASPICE CL2, guaranteeing the highest software quality through certified development processes and through quality assurance on all process and development steps
- Guaranteed, high-quality, low-latency support on current and old compiler versions so your development never stalls
- No third-party code in the C-compiler toolchain – all issues can be handled quickly in-house
- Compiler toolchain safety kit that makes it easy to qualify and certify the compiler toolchain for your safety project
- Tools to optimize performance vs. code size

- Tools to establish freedom from interference (FFI) between software components with different ASIL levels, per Chapter 7 of ISO 26262.

Performance; You should look for more than a compiler that "just works." Instead, choose a compiler that benefits from its vendor's undivided attention. Many embedded compilers are based on open source technology such as gcc or LLVM. This can be an advantage when addressing high-end cores from Intel, Cortex-A, and similar vendors. From a compiler perspective, the performance-relevant characteristics of these architectures are similar. Speed is typically determined by the following:
- Cache hierarchy (memory is much slower than the core and caches prevent the core from constantly waiting for memory) – see the discussion of the Intel Haswell and ARM v-8A architectures
- Efficient exploitation of the single instruction, multiple data (SIMD) units or floating-point units (FPUs)
- Other special-purpose instructions.

These high-end cores perform out-of-order execution, advanced branch prediction, register renaming, and many other tricks to improve throughput, which substantially lessens the pressure on the compiler in terms of pipeline optimizations. Many optimizations and algorithms in the frontend and backend of LLVM are tailored toward these kinds of high-end cores. Porting code to a new core with similar characteristics can be as simple as adapting a few key values such as cache sizes; the instruction set does not change.

Addressing complex embedded multicore processors such as the Infineon AURIX TriCore is dramatically different, because these processors are radically different from high-end cores. Often these embedded cores combine features from digital signal processing (DSP), reduced instruction set computing (RISC), very long instruction word (VLIW), and special accelerator hardware such as the FFT unit.

Many algorithms from the existing LLVM backends are not easily adapted for complex embedded devices like these, meaning that the backend for such a device needs to be written almost from scratch. Because many of the performance-relevant optimizations for such complex embedded devices occur in the backend rather than the frontend, there is little benefit from using the LLVM framework to create high-performance code on an AURIX device. You are no better off than starting with a completely new compiler using a frontend of your choice.

STEP 3: DEVICE CONFIGURATION

Multicore processors are extremely powerful devices. There are hundreds of variants with different functional configurations. For example, a single AURIX device can contain up to six TriCore cores, a hardware security module (HSM), a generic timer module (GTM), and a host of peripherals.
You must write the startup code that correctly configures clocks, memory, and peripherals. An extensive manual is provided with each core, outlining pin constraints and peripheral configuration options – which all must be considered to create a valid pin mapping.

The following sections of this article continue to consider; Benchmarking; the Software Platform; Fine-tuning your application; Memory layout; and One size fits all – position-independent modules. Click the panel below for full pdf.

Download PDF of Article

Find Automotive Coding on EETsearch

5G CHALLENGES DEMAND A NEW KIND OF PROCESSOR

By Emmanuel Gresset, CEVA

The move to the 5G suite of standards for cellular communications is about much more than delivering faster download speeds to mobile users. It's a change that demands a rethink of the way infrastructure equipment is designed.

5G represents a massive expansion in the capabilities of wireless networking, extending services to new markets ranging from forests of environmental sensor nodes up to self-driving vehicles, multiuser virtual reality (VR) interfaces and Enhanced Mobile Broadband (eMBB) services such as 4K video streaming.

5G supports use-cases that are not possible with existing standards such as LTE and LTE-A Pro (Gigabit LTE). It will connect fast-moving cars to each other and to cloud-based services that provide traffic updates, live entertainment and vital safety data. Just within that use-case is a need for high data rates coupled with extremely low latency. The standards call for a five-fold reduction in average latency and for the ability to handle as many as a million low-data rate devices within a single cell.

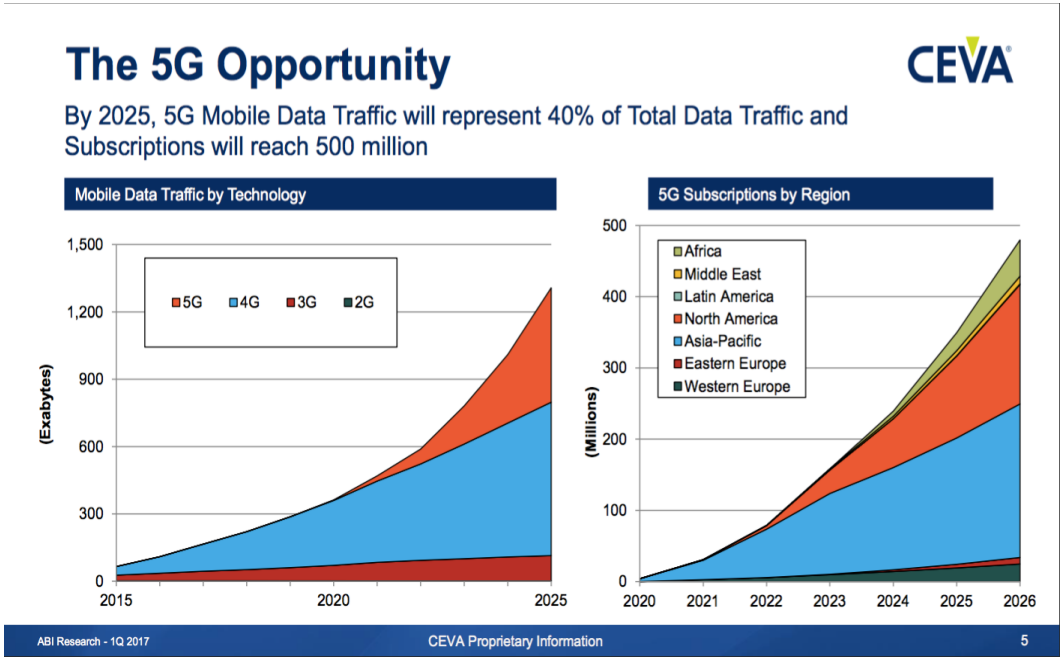


Figure 1. *5G market opportunity (Source: ABI research)*

Delivering the bandwidth and responsiveness to handle these new applications presents infrastructure equipment builders with a huge challenge.

To support eMBB services and the need for data rates of 1 Gbit/sec per wireless user or more anywhere in the world, 5G introduces a number of novel requirements. It needs infrastructure able to adapt easily to a wide range of frequency bands – from 400 MHz all the way up to 80 GHz. Base stations will need to use multi-RAT (-radio access technology) aggregation, called Non Standalone (NSA) mode in 5G, to process and control data sent using different channels and protocols. NSA aggregates LTE control or anchor channels in sub 3.5GHz bands with high data rate channels based on 5G NR (New RAT) from 3.5 GHz bands all the way to mm waves. Massive MIMO architectures will make it possible to accommodate multiple high-data rate users within a single cell.

NEW TECHNIQUES NEED NEW CAPABILITIES

Techniques such as massive MIMO demand new capabilities from hardware. Phase noise becomes critical in key protocols envisaged for 5G, such as those used for mm-wave communications above 6 GHz frequency bands that employ higher order modulation schemes such as 256-QAM and up. The algorithms to overcome issues introduced by phase noise demand higher precision floating-point arithmetic than has been the case with prior standards. It

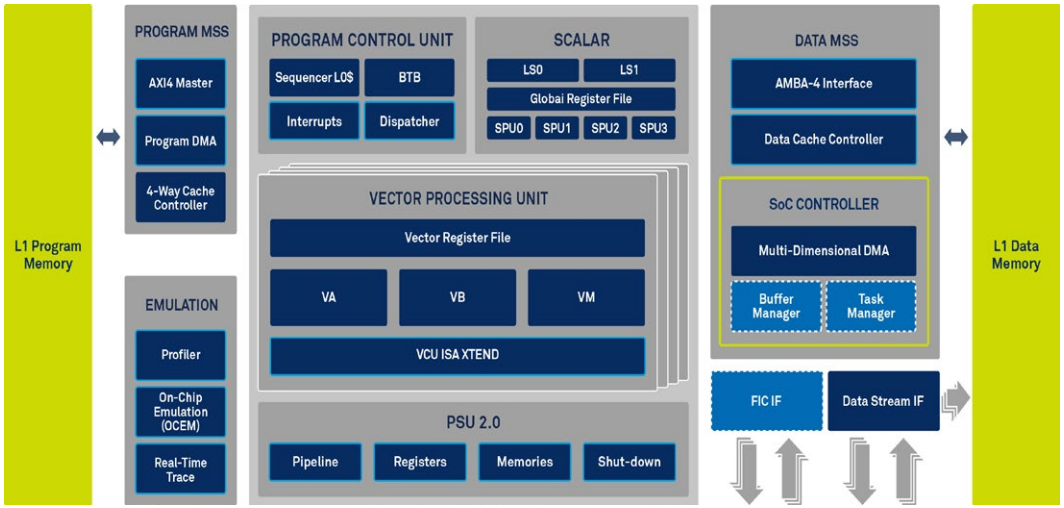


Figure 2. *CEVA-XC12 processor architecture*

is also not enough to optimize for multiplication throughput in the hardware that supports massive MIMO. The algorithms call for the ability to perform operations such as matrix inversion efficiently. As a result, non-linear operations such as high-speed division and square-root functions are required.

Because of the data rate increases and associated changes in modulation and channel processing, each step of the receiver and transmit chain calls for greater speed. Receive-chain tasks such as channel estimation, equalization and estimating noise covariance each double in their computational requirements.

The increased complexity that comes with 256-QAM and more complex modulation schemes leads to an increase in computational overhead of as much as eight-fold for tasks such as demapping. The need for 1 msec response latency to service mission critical and autonomous control applications means a 4x increase in the performance needed for the HARQ (hybrid automatic repeat request) module to ensure data is retransmitted in a timely manner and to process the more complex forward error correction algorithms.

The high throughput requirements on their own could be serviced by a hardware-intensive implementation. But this will not readily satisfy the requirements for successful 5G systems. Flexibility and adaptability are key to a successful 5G infrastructure strategy. Each base station location will have a different set of needs that cannot readily be supported by fixed hardware configurations. And in the short term, standards will evolve as trials uncover issues and interactions between the many different components needed to support high throughput.

ARCHITECTURAL REQUIREMENTS

There is a clear demand for an architecture that combines hardware acceleration and efficiency with the programmability of software. For example, the FFT and IFFT functions needed to process signals close to the antenna are always required so can be readily implemented in a hardware accelerator. But functions such as receive control require the flexibility of software.

The stringent latency requirements of 5G call for the ability to reorder channel-processing tasks quickly as demands change. This leads to much higher scheduling complexity compared to prior base station architectures. Although high computational capacity is a clear requirement, performance cannot simply be optimized for dataplane throughput. Control-plane efficiency is more critical than ever and points to the need for extensive software programmability but implemented in a way that satisfies the low-energy requirements of 5G implementations.

Scalability is a further requirement to satisfy the need for many base station configurations derived from a single architecture. This will allow OEMs and integrators to build equipment that can be tuned for deployments that range from indoor residential and enterprise environment femtocells to small cells in the dense urban environment that favour the use of mm-wave and Wi-Fi protocols through to macrocell and Cloud RAN units that fully leverage massive-MIMO technologies.

Efficient multiprocessing provides the key to

such scalability. In contrast to traditional multiprocessing architectures that force traffic through an interconnect such as AXI, the CEVA-XC12 processor architecture exploits high-bandwidth point-to-point fast interconnect (FIC) channels. Using these channels, each processor can write results of computations directly into the memory or cache of its neighbours without placing any demand on the AXI matrix and avoid L2 cache overhead to load and store data buffers. Queue and buffer managers offload the transfers themselves from the DSPs to help maximize instruction throughput.

The multiprocessing architecture with FIC makes it possible to use multiple cores to share the workload for high-overhead tasks such as channel estimation or data-symbol processing. Cores can easily exchange intermediate results to support the creation of channel estimates for groups of receive antennas and provide equalization information for multiple subcarriers.

To provide the high DSP power required for algorithms such as demodulation, demapping and MIMO processing and beamforming, the XC12 deploys a set of multiply-accumulate engines in its quad vector unit that can execute as many as 128 in parallel with high precision arithmetic – representing, on average, a three fold boost in performance over previous generations.

Each of the execution units in the XC12 supports 20-bit floating-point arithmetic. The increased precision this offers compared to previous processor implementations improves the signal-to-noise ratio by up to 30 dB for massive-MIMO and mm-wave processing tasks. Trigonometric instructions boost the speed of 256-QAM demodulation. Similarly, instruction extensions designed for generating pseudorandom bit sequence (PRBS) patterns help boost descrambling throughput by a factor of three.

The complex scheduling requirements of 5G are supported by the CEVA-X scalar processing unit (SPU) used in the XC12. The XC12 supports four identical SPUs that coordinate both control and DSP capabilities in the system. The optimization for complex control tasks is reflected in the SPU's performance on the EEMBC CoreMark benchmark, achieving a 40% improvement over its predecessor, the CEVA-XC4500, for a score of 4.4.

The SPU supports ultra-fast context switching between tasks and includes a number of features to enhance responsiveness when handling branch-intensive control software. The SPU incorporates a branch-target buffer that works with a dynamic branch prediction unit to remove the stalling effect of branches encountered with traditional DSP architectures.

Throughput is further enhanced through the use of a non-blocking level-zero instruction cache with automatic prefetch, coupled with a level-one instruction cache that employs a four-way set-associative structure that keeps frequently used instructions in the cache subsystem for longer than simpler direct-mapped designs.

The result of the combination of features in the XC12 is a balanced architecture that fully supports the demands of forthcoming 5G infrastructure equipment projects, with the ability to scale from femtocell designs up to large-scale massive MIMO-enabled macrocells and Cloud RAN.

Emmanuel Gresset *is a Business Development Director in CEVA's Wireless Business Unit. For the last 30 years, Mr. Gresset has been with systems and semiconductor companies working in the fields of signal processing, wireless modems as well as processor and system-on-a-chip architecture in various companies: Octasic, STMicroelectronics, Philips, VLSI Technology, Spectral Innovations and Thomson. He received his M.Eng from the Ecole Supérieure d'Electricité in Paris.*

www.ceva-dsp.com

Find 5G Signal Processing on EETsearch

MICRO-OHMS MAKE THE DIFFERENCE IN MOSFETS FOR CRITICAL AUTOMOTIVE APPLICATIONS

By Georges Tchouangue & Eiji Shimada, Toshiba Electronics Europe

The amount of electronic content increases in modern vehicles. In their role as power switches, MOSFETs must realise higher power densities and increased thermal performance that enable designers to realise their target functionality, reliability and robustness in a limited space. In this article, we look at the evolution of DPAK and D2PAK class automotive power MOSFETs and show how the latest advances in packaging and processes are addressing today's demanding automotive applications.

MOSFET requirements vary depending on the specific use case, and the location in the vehicle, which defines the level of ruggedness and thermal performance requirement. Leading semiconductor manufacturers provide a suite of products to designers that offer multiple options in terms of electrical performance and thermal performance through a variety of package types. To be suitable for the challenging automotive environment, these MOSFETs need to be qualified to relevant automotive standards such as AEC-Q101.

As more functions in vehicles become electrified, then the number of power devices deployed in the vehicle rises in proportion. Vehicle voltages are rising from 12V through 24V to 48V, increasing the demand for 100V MOSFETs. Finally, in the increasingly dense spaces within modern vehicles, ambient temperatures are higher than in consumer, computing or even industrial applications. This brings a significant challenge to system designers as there is less margin for temperature rise in the device.

THE CHALLENGES: ELECTRICAL AND THERMAL PERFORMANCE

Semiconductor companies have two main thrusts in addressing these challenges; electrical and thermal. From an electrical perspective, semiconductor performance constantly improves, along with the associated wafer technology to reduce resistances and capacitances in the final device. These improvements bring greater efficiencies and allow for faster switching, delivering MOSFETs suitable for today's high-power-density applications.

In parallel with this, package technology is the subject of significant development effort. The need to reduce ECU (Electronic Control Unit) size can be achieved with significantly smaller MOSFET packaging. The challenge is how to realize the same level of thermal performance in these smaller spaces. Companies are seeking increasingly innovative ways to transfer heat from the semiconductor junction, thereby enabling the greater thermal efficiencies required for space-constrained high-power systems operating at elevated ambient temperatures.

As a company that has been developing automotive power MOSFETs for many years, Toshiba has assembled a portfolio of automotive power MOSFETs that encompasses N-channel and P-channel devices (the latter are particularly useful for reverse battery protection) based on trench gate technology, which can offer an optimised combination of conduction and switching performance in the target voltage range.

INNOVATION IN PACKAGE TECHNOLOGY

Package technology has a huge impact on reliability and the ability to support higher currents within high-power automotive applications.

In traditional power MOSFET packages, the wire bonds from the die to the lead frame limit current-carrying capability, and also represent a common point of failure. In order to address these limitations, Toshiba has developed an alternative bonding technology.

Believed to be unique amongst automotive power MOSFET suppliers, this approach uses copper connectors (that is, copper clips)

in large power packages such as DPAK and D2PAK, as opposed to conventional aluminium wire bonding. Toshiba launched a copper connector based TO-220SM(W) package as early as 2008 - this is the original 10 x 13 mm SMD (Surface-Mount-Device) automotive power package. Copper connectors for automotive DPAK (TO-252) and D2PAK (TO-263) followed in 2011 and 2015, the advanced packages being designated DPAK+ and D2PAK+ to distinguish them from wire-bond packages.

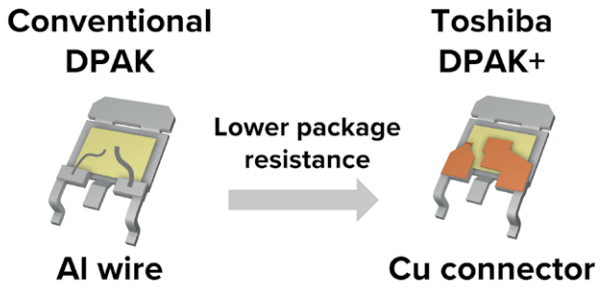


Figure 1. *DPAK+ and D2PAK+ include copper connectors that contribute to a reduction in package resistance and thereby heat generation.*

The copper connector delivers multiple benefits, especially in automotive applications. Firstly, the contact area between the source pad and source copper connector is significantly increased, leading to less planar current on the source pad metal layer. Copper conductivity is much better than aluminium, both electrically and thermally. Thermal conductivity is 401W/(m·K) for copper, while it is 237W/(m·K) for aluminium. Electrical resistivity (at 20°C) is 16.8 nΩ·m for copper and 28.2 nΩ·m for aluminium. Increased thermal conductivity moves heat more quickly from the connector element of the package and the lower resistivity contributes to the reduction of package resistance, thereby reducing heat generation.

To demonstrate and utilise the benefits of the copper connector technology, Toshiba developed the unique TO-220SM(W). This 10 x 13 mm SMD power package appears similar to a 10 x 15 mm D2PAK (TO-263). On closer inspection, it can be seen that the TO-220SM(W) has much shorter and 3x wider source pin than a normal D2PAK package (Figure 2).

Figure 2. *TO-263 and the advanced TO-220 SM (W) package compared.*

COMPARING MOSFET ON-RESISTANCE

Due to the changed source pin dimensions, package resistance is reduced by about 0.15 mΩ (150 µΩ). If we compare the TK1R4F04PB 40V, 1.35 mΩ (max) MOSFET in the TO-220SM(W) package with the TK1R5R04PB 40V, 1.5 mΩ (max) MOSFET in D2PAK+, the improvement is apparent. While both devices are based on the same chip, the on-resistance (RDS(ON)) of TK1R4F04PB is 0.15 mΩ lower than that of the TK1R5R04PB. Even a small improvement of 0.15 mΩ is very significant with RDS(ON) values of a few milliohms. The TK-74F04PB is a 40V MOSFET in the TO-220SM(W) package with an RDS(ON) of 0.74 mΩ (max). This extremely low value can only be achieved by the combination of the copper connector technology, the TO-220SW(W) package technology, and an advanced wafer process.

This article concludes by summarising further critical aspects of automotive MOSFET performance, such as switching behaviour for parallel device operation; click panel below for full pdf.

Download PDF of Article

Find Automotive MOSFETS on EETsearch

productroundup

productroundup

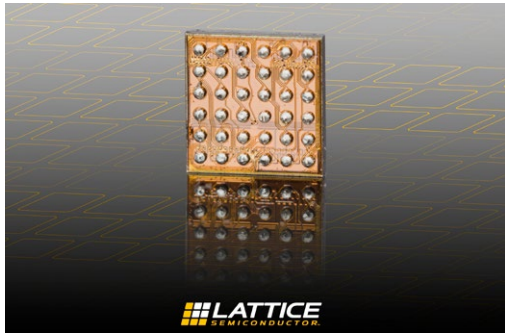
TinyCircuits' mini open-source functional blocks

Distributor Digi-Key now has TinyCircuits' small-size open source electronics, including the TinyDuino, an Arduino-compatible platform the size of a €2 coin. The TinyDuino platform is modular and provides tiny electronic building blocks, so users can easily add complex functions, such as GPS, Wi-Fi, motor control, or graphics displays to projects by plugging the expandable modules (called TinyShields). Applications include Maker projects, IoT, prototyping, and educational learning.

Complete article, here

IP cores enable video bridging functions in FPGA

Lattice Semiconductor is developing its CrossLink series of IP for its programmable logic devices, with seven modular IP cores for video bridging capabilities across consumer, industrial and automotive applications; the IP supports image capture and display applications for delivering AR/VR, embedded vision and other intelligence-at-the-edge products. The IP is for the CrossLink FPGA range. The latest cores include: CSI-2/DSI D-PHY Rx/Tx; FPD-LINK Rx/Tx; SubLVDS Image Sensor Receiver; Pixel to Byte Converter; and Byte to Pixel Converter.



Complete article, here

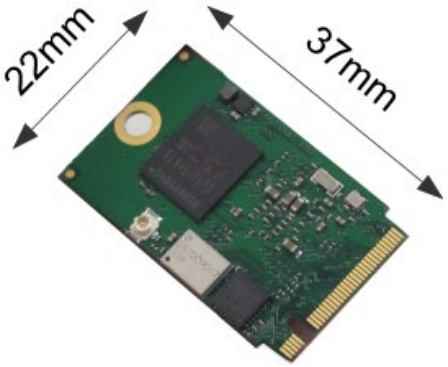
Power inductor terminations aid AOI & 3D PCB builds

High current, moulded, power inductors from Coilcraft have special termination options that simplify automated optical inspection (AOI) of the component during the solder reflow process. The range offers inductance values from 10 to 47 µH – significantly higher than alternative products in the same size part. It also provides current handling up to 5.3 Amps and very low AC + DC power losses for greater efficiency. XTL7030 inductors measure 7.1 mm square, with a maximum height of 3.2 mm. They are also qualified to AEC-Q200 Grade 1 standards.

Complete article, here

System-on-module is smallest embedded i.MX6ULL

Armadeus Systems' latest System On Module in the OposSOM family: the OPOS6UL_NANO is aimed at industrial domains such as IOT, drones, medical devices and industrial controllers. With a size of 22 x 37 mm the OPOS6UL_NANO uses a form factor derived from the M.2/NGFF standard suiting it for portable systems. It hosts an NXP i.MX6ULL/iMX6UL processor (Cortex A7 core) using a clock frequency between 528MHz and 900MHz, to which is added 256 to 512 MBytes DDR3L 800MHz, a 4 GB to 32 GBytes eMMC, and Ethernet PHY.

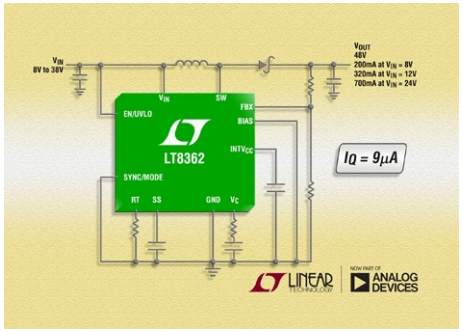


Complete article, here

productroundup

2A, 2MHz, 60V multi-mode step-up DC/DC, 9µA I_Q

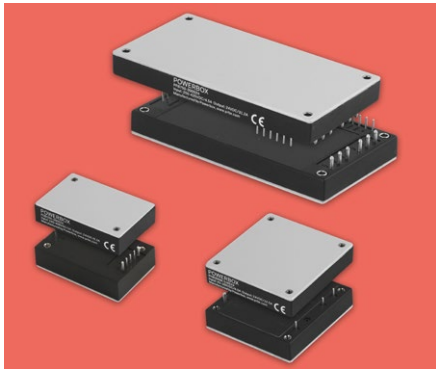
LT8362 is a current mode, 2-MHz step-up DC/DC converter with an internal 2A, 60V switch. It operates from an input voltage range of 2.8V to 60V, suitable for applications with input sources ranging from a single-cell Li-Ion battery to automotive and industrial inputs. The converter can be configured as either a boost, SEPIC or an inverting converter. Its switching frequency can be programmed between 300 kHz and 2 MHz. It offers over 90% efficiency switching at 2 MHz. Burst Mode operation reduces quiescent current to 9 µA while keeping output ripple below 15 mV_{P-P}.



Complete article, here

Powering datacentres & 'microgrids' from HV DC buses

Swedish power-conversion company Powerbox has designed a range of high input voltage DC/DC converters for microgrids and datacentres and industrial applications. Part of its industrial line, the new series of HVDC/DC converters operate with an input voltage range of 180VDC to 425VDC, and deliver output power levels from 150W to 750W. The PQB-PHB-PFB300S series is built around a high efficiency topology, with a layout optimized for thermal conduction, an input/output isolation of 3,000VAC minimum and deliver output voltages from 3.3 VDC to 48 VDC.



Complete article, here

16-ch data acquisition IC; 14-bit, bipolar input, dual simultaneous sampling ADC

Analog Devices (ADI) has released the AD7617, a 14-bit, DAS (data acquisition system) that supports dual simultaneous sampling of 16 channels. The AD7617 operates from a single +5V supply and can accommodate ±10V, ±5V, and ±2.5V true bipolar input signals while sampling at throughput rates up to 1 Msample/sec per channel pair with 85 dB signal-to-noise ratio (SNR). Higher SNR performance can be achieved with the on-chip oversampling mode (85.3 dB for an oversampling ratio (OSR) of 2). The input clamp protection circuitry can tolerate voltages up to ±21V. The AD7617 has 1 MΩ analogue input impedance, regardless of sampling frequency. The single-supply operation, on-chip filtering, and high input impedance eliminate the need for driver op amps and external bipolar supplies.

Complete article, here

Differential current sensor IC combines accuracy & 4.8 kV isolation

Allegro MicroSystems' latest differential, high isolation current sensor IC has integrated, low power conductors and up to 4800 VRMS galvanic isolation, with user settable over-current fault outputs. The ACS720 works off a single 5V supply while maintaining an output voltage swing from 0 to 3V, with a stable zero current output of 1.5V. This allows the ACS720 to operate off a 5V supply while having an output which is compatible with typical 3.3V ADCs found on many MCUs. ACS720's high PSRR rejects the noise often found on the supplies in the power section of the PCB or system.

Complete article, here

productroundup

100W, 1/32nd-brick-outline DC-DC converters

TDK's 100W i3A series of non-isolated DC-DC converters is packaged in the industry standard 1/32nd brick form factor. These step-down converters are capable of adjustment from either 3.3 to 16.5V or 5 to 30V output and accept an input voltage of 9 to 53V. The i3A series can be used to derive additional high power outputs from a single output 12V, 24V, 36V or 48V supply, at lower cost than traditional isolated DC-DC converters. With efficiencies of up to 98%, these compact converters measure 19.1 x 23.4 x 9.6 mm and can operate in ambient temperatures of -40°C to +125°C.

Complete article, here

Wireless power demo kit sends 33W

Employing its own gallium nitride (GaN) FETs, Efficient Power Conversion Corporation (EPC) has configured a complete class 4 wireless power charging kit, the EPC9120. The system can transmit up to 33 W while operating at 6.78 MHz (the lowest ISM band). The purpose of this demonstration kit is to simplify the evaluation process of using eGaN FETs for efficient wireless power transfer. The EPC9120 utilizes the high frequency switching capability of EPC gallium nitride transistors to facilitate wireless power systems with full power efficiency between 80% and 90% under various operating conditions.

Complete article, here

Voice capture kit accesses Alexa Voice Service

Distributor Digi-Key has Cirrus Logic's Voice Capture Development Kit for Amazon AVS, a complete solution for developing a hands-free AVS product enabled with Alexa, Amazon's intelligent voice control service. The kit features Cirrus Logic's SoundClear voice capture solution, smart codec, MEMS microphones, and control console that makes use of the AVS APIs to help developers, design engineers, and OEMs build commercial-grade, voice-activated products, for sectors such as portable smart speakers, networked smart speakers, digital assistants, and smart home voice control.

Complete article, here

High-side, 76V current sense amp uses small shunts

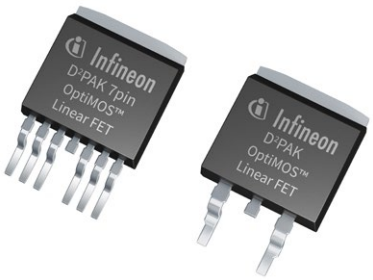
Maxim Integrated's MAX40010 is a single-channel high-side precision current- sense amplifier with an input common-mode voltage range from 2.7V to 76V. The device has accuracy specifications of less than 12 µV (max) input offset voltage and less than 0.1% (max) gain error. By offering precision offset and gain error specifications, the MAX40010 makes it possible to sense very small sense/shunt resistors, improving system efficiencies and power dissipation through the sense element. The MAX40010 features 80 kHz of small signal bandwidth and four unique gain options (12.5V/V, 20V/V, 50V/V, and 100V/V). The device's current sense inputs have EMIR filters to reject RF found in communications equipment. The MAX40010 operates over the -40° C to + 125°C temperature range and comes in a 6-bump, 1 x 1.5 mm wafer-lever package (WLP) with 0.5 mm pitch and a SOT23 U6SN+1 package.

Complete article, here

productroundup

Linear FET combines low RDS(on) with large SOA

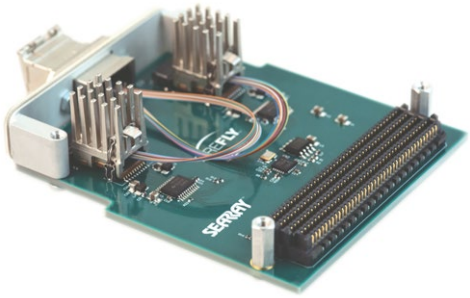
Infineon's 100V, 150V, and 200V OptiMOS Linear FET series combines the on-state resistance (RDS(on)) of a trench MOSFET with the wide safe operating area of a planar MOSFET. This solves the trade-off between RDS(on) and linear mode capability. The OptiMOS Linear FET can operate in the saturation region of an enhanced mode MOSFET. It is suited for hot-swap, e-fuse, and protection applications commonly found in telecom and battery management systems (BMS). The OptiMOS Linear FET prevents damage at the load if there is a short circuit, by limiting high in-rush currents.



Complete article, here

FPGA-to-fibre with Samtec's 14 Gbps FireFly FMC kit

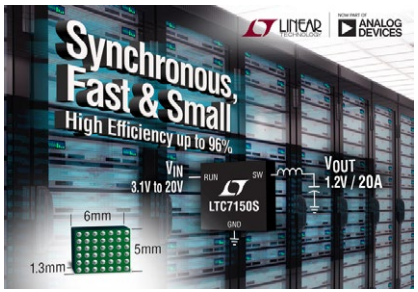
Providing simplified connections between FPGAs and fibre optics, Samtec has released the 14 Gbps FireFly FMC development kit to provide an easy-to-use evaluation and development platform for Samtec's FireFly optical engines. The FMC Module provides up to 140 Gbps full-duplex bandwidth over 10 channels from an FPGA to an industry-standard multi-mode fibre optic cable. The kit supports Data Centre, High Performance Computing and FPGA-to-FPGA protocols including Ethernet, InfiniBand, Fibre Channel and Aurora, supporting cable lengths up to 100m.



Complete article, here

20V, 20A monolithic synchronous buck regulator

LTC7150S is a 20V, 20A monolithic synchronous buck converter with differential V_{OUT} remote sensing. The device's phase-lockable, controlled on-time constant frequency current mode architecture eases compensation and is suitable for high step-down ratio applications that operate at high frequencies while demanding fast transient response. Its 3.1V to 20V input range supports a wide variety of applications, including most intermediate bus voltages, and is compatible with many battery types. Integrated N-channel MOSFETs deliver continuous load currents as high as 20A at output voltages from 0.6V to V_{IN}.



Complete article, here

32 x 8 x 2.75 mm power-on-package targets high-current processors

Vicor's Power-on-Package modular current multipliers are aimed at high performance, high current, CPU/GPU/ASIC ("XPU") processors running at hundreds of Amps. As current multipliers, MCMs mounted on the XPU substrate under the XPU package lid, or outside of it, are driven at a fraction (e.g., 1/64th) of the XPU current from an external Modular Current Driver (MCD). The MCD, located on the motherboard, drives MCMs and accurately regulates the XPU voltage with high bandwidth and low noise. Two MCMs and one MCD, can deliver up to 320A of continuous current, 640A peak.

Complete article, here

eeDesignNews EUROPE

CONTACTS

PUBLISHER

André Rousselot
+32 27400053
andre.rousselot@electronicseurope.net

EDITOR-IN-CHIEF

Graham Prophet
+44 7733 457432
graham.prophet@electronicseurope.net

CIRCULATION & FINANCE

Luc Desimpel
luc.desimpel@electronicseurope.net

ADVERTISING PRODUCTION & REPRINTS

Lydia Gijsegom
lydia.gijsegom@electronicseurope.net

ART MANAGER

Jean-Paul Speliers

ACCOUNTING

Ricardo Pinto Ferreira

SALES CONTACTS

Europe

Germany,
PLZ 0 1 2 & 7 8 9
Marcus Plantenberg
+49 (0) 89 5507 9909
m.plantenberg@pms-plantenberg.de

Germany,
PLZ 3 4 5 6
Karin Weisshaupt
+49 (0) 613 1329 1444
KAROMedienservice@email.de

UK, Ireland, Israel,
The Netherlands
Nick Walker
+44 (0) 1442 864191
nickjwalker@btinternet.com
Julie Afford
+44 (0)7717 117631
Intladsales@gmail.com

Switzerland, Austria
Monika Ailinger
+41-41-850 4424
m.ailinger@marcomedia.ch

Italy
Andrea Rancati
+39-02-70300088
arancati@rancatinet.it

Scandinavia
Colm Barry & Jeff Draycott
+46 (0)413 251111
jeff.draycott@womp-int.com
colm.barry@telia.com

France, Spain, Portugal
Daniel Cardon
+33 688 27 06 35
cardon.d@gmail.com

Belgium
Nadia Liefsoens
+32-11-224 397
n.liefsoens@fivemedia.be

USA & Canada

West
Twyla Sulesky
+1 408-779-0005
tsulesky@aceadpro.com

PA, NJ & NY
Jim Lees
+1-610-626 0540
jim@leesmedia.com

East, Midwest, South Central & Canada
Steve Priessman
+1-352 325-4100
steve@stevenpriessman.com

East, Midwest, South Central & Canada
Lesley Harmoning
+1-218.686.6438
lesleyharmoning@gmail.com

Asia

Japan
Keita Sato
+81-3-6824-9386
ksato@mx.itmedia.co.jp

european business press

eeDesignNews-EUROPE is published 11 times in 2017 by
European Business Press SA, 533 Chaussée de Louvain, 1380 Lasne, Belgium Tel: +32-2-740 00 50 Fax: +32-2-740 00 59
email: info@electronicseurope.net - VAT Registration: BE 461.357.437. - RPM: Nivelles.
It is is free to qualified engineers and managers involved in engineering decisions – see: http://www.eedesigneurope.com/subscribe