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imec, in collaboration with Vrije Universiteit Brussel, Brussels, has succeeded in producing 79 GHz radar transmitter signals using only “plain digital” 28 nm CMOS, paving the way towards full radar-on-chip solutions for automotive and smart environment applications. Read the news item on page 7.

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The assertion that there is an issue around security, in the coming connected world that is promised to us as the Internet of Things, is beyond dispute. It’s also true, as has often been stated in other contexts, that there’s no such thing as absolute security. Security comes with a price tag, in both directions – creating it or breaking it. The task becomes spending an acceptable amount of money and effort on the “good guys” side of the equation, to set up a level of security that is too costly for the “dark side” to consider worth attacking.

Even the most superficial look at what lies ahead indicates some areas of the problem. You can pick your own figure for the number of connected devices that we will have in the world by, say, 2020 – there is no shortage of forecasts, from the modest-billions to improbably-big-billions; but billions, anyway. Even if all of those designed from tomorrow onwards were to incorporate immaculate and seamless security, the IoT will absorb unknowable numbers of devices that are around today, that have been designed with a level of attention to security that will range upwards from none-at-all. Vulnerabilities are, in other words, built in to the IoT, version 0.5, before we even get started.

The subject was addressed in the Conference Keynote address to the 2014 embedded world event in Nuremberg, in February, given by David Kleidermacher, of Green Hills Software. We need, he said, an improved strategy as a base to proceed; how we think of security and how we go about implementing it. If a billion connected objects sounds challenging, “think what happens when there is a trillion, all plucking valuable information out of the environment.”

One of Kleidermacher’s starting points is what he terms the Myth of Centralisation; that the security problem can be tackled if we, “lock down the servers” - in the view in which the IoT consists of centralised, powerful servers, surrounded by and connected to the “things”. We already have the best security we can contrive, applied to server farms; they are buried in subterranean bunkers, so are physically protected; they are surrounded by layers of hardware and software network protection, yet serious data breaches still occur. The edge of the network is poorly protected; “There are two parts to the Myth; [firstly] that you don’t need to protect the Thing because the centre is what’s really important. But if you’re a hacker, you are going to go after the weakest link: if we fail to protect the Thing, the hacker will go after the Thing, and use it as a conduit to get to the server.” The second part of the Myth is that no useful information is left in the edge – it is all accredited to the centre. “That is not true today and is really not true in the future. In the coming decades all sort of truly valuable information is going to be out there.” This, Kleidermacher reflects, is how the Target [US retail store chain] customer-data theft was executed – by placing malware into a point-of-sale system.

On the same principle, Kleidermacher anticipates bot-net style attacks, carried out using the IoT, if you are going to compromise computing devices to your own ends; do you go after the [relatively speaking, protected] PCs, (there could be a billion of them) or do you use the things that may be less intelligent, but may also be less protected, at the edge – where there is a trillion of them?

I have insufficient space in this column to report more than a few details of David Kleidermacher’s prescription to forestall a security nightmare, but it actually involves few totally novel concepts. For example; apply minimum-necessary privileges. That is, give actors and systems access only to the resources they need for their function – and no more. Build systems of elegance and minimum-needed complexity that can be (independently) demonstrated to be secure. Apply componentisation and virtualisation to limit reach and access (of systems). Establish secure software development (“white room”) practices, and build methodologies to get secure software for manageable costs. None of this – and there is far more – is fundamentally new, other than in the fact of applying it to systems on the scale of IoT Nodes.

There is some good news to be had here; David Kleidermacher (as you might reasonably expect of the CTO of a company with a deep interest in the success of the concept) believes that it can be done: we can have a connected world with an acceptable degree of security. Not least because, as with so many other fields, semiconductor integration gives to small systems, the resources needed to run the encryption and added supervisory layers that will be needed. There is no room in the Internet of Things, he concludes, for IDIOTS.

IDIOTS? - that would be, “Insecure Devices on the Internet of Things.”

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Cree doubles light output from high-density LED arrays

Cree’s latest CXA high-density LED arrays enable, the company says, the basis of new designs and applications for LED lighting. Three new LED arrays – the XLamp CXA2590, CXA1850 and CXA1310 High-Density LED Arrays – double the light output of existing standard-density CXA LED arrays without increasing the size. This increase in lumens delivers new levels of light intensity, which enables the complete replacement of ceramic-metal-halide (CMH) light sources, expands the possibilities of LED spotlights and enables applications that could not be addressed by previous LED technologies.

By emitting more than 15,500 lumens from a 19-mm light source, the CXA2590 LED Array enables luminaires with the same centre-beam candlepower (CBCP) and light quality of a 150-W CMH light source at lower power level, with longer lifetime and with better control. Delivering more than 9,000 lumens from a 12-mm light source, the CXA1850 LED Array enables lighting solutions with the same CBCP and light quality as 70-W CMH while using half the power. The CXA1310 LED Array provides more than 2,000 lumens in a 6-mm light source, which allows lighting manufacturers to design smaller, more-efficient track lights, reduce the size of halogen replacements by half and deliver twice the CBCP of CMH at 30% less power.

Offering optimum colour consistency for designs that use only one LED, Cree XLamp CXA LED Arrays are characterised and binned at 85°C, available in ANSI White and EasyWhite colour temperatures (2700 K – 6500 K), and CRI options of 70, 80 and 95.

Model-based design finally gets an embedded tool chain

BY NICK FLAHERTY

Two European companies have joined forces to provide what they believe to be the first full tool chain for high level model-based design in embedded systems. Model-based tool provider LieberLieber Software is working with debug tool chain developer iSystem on an integrated tool chain for model based testing and debugging of embedded software. This cooperation allows software developers to use UML-tools to test and debug on the model layer.

Both the market for embedded solutions and the market for model based software and system development are growing, but there is a lack of tools for testing and debugging software directly from the model with specific hardware. “The embedded market finally is ready. It took some years to bring modeling, code generation and debugging tools together,” said Erol Simsek, CEO of iSystem.

The tool chain combines the enar uml debugger, the first graphical UML debugger integrated in Enterprise Architect, with winIDEA, an integrated development environment for embedded software development and testing. LieberLieber’s UML debugger is based on enar uml2code, a code generator for embedded systems. The code generated by a customer-selected compiler may be transferred directly to the hardware. Finally enar uml debugger is connected to the target system through iSystem’s infrastructure, allowing graphical testing of code and debugging of the model with the visualisation module of the UML debugger. Both code generator and UML debugger from LieberLieber Software support class and activity models as well as state machines. iSystem’s software and hardware tools (winIDEA and blue box) are available for more than 50 different CPU architectures, 3500 microcontrollers and 150 compilers.

“Together we address the growing market of model based embedded development and provide an integrated tool chain for testing and debugging embedded software”, says Roman Bretz, CTO of LieberLieber Software. “Efficient model based approaches to embedded software development need to build on an integrated tool chain. Our first step on the embedded market was the enar uml2code for embedded systems, a code generator providing platform independent C++ and MISRA compliant C-code from UML models. With the enar uml debugger we expand our offer for the embedded market and the cooperation with iSystem is a major step on this way. Our partner addresses a wide variety of microcontroller platforms, allowing developers to test and debug their software on the target platform,” he said.

The combination of winIDEA, the embedded software development platform; the blue box from iSystem; and LieberLieber Software’s enar uml debugger, make possible a new tool chain for the Enterprise Architect community.

iSystem;
www.isystem.com
28-nm “digital” CMOS generates 79 GHz radar signals – will enable radar-on-a-chip

Imec, in collaboration with Vrije Universiteit Brussel, Brussels, has succeeded in producing 79 GHz radar transmitter signals using only “plain digital” 28 nm CMOS. With an output power above 10 dBm, the transmitter front-end paves the way towards full radar-on-chip solutions for automotive and smart environment applications.

Millimetre-wave radar systems potentially offer range resolution finer than 10 cm and an angular resolution finer than 10 degrees, and will be used in next-generation driver assistance systems to improve safety in poor-visibility conditions (dust, fog, and darkness) where image-based driver assistance systems fail. Conventionally, the high bandwidth and carrier frequency needed to achieve such high resolution, wide field of view and high angular resolution, translate into large, expensive and power hungry mm-wave antenna arrays. A low power compact radar technology, imec believes, will be key to enable the application of mm-wave sensors in next generation automotive and smart environment applications.

Imec’s continuous wave (CW) radar transmitter operates in the 79 GHz band. Implemented in 28 nm CMOS, with a supply voltage of 0.9V, it only consumes 121 mW and is fully compliant with the spectral mask imposed by ETSI. Phase modulation guarantees high resilience against interference and enables code-domain multiple-input, multiple-output (MIMO) radar.

These results were presented at the recent ISSCC2014 (San Francisco): “A 79GHz phase-modulated 4GHz-BW CW Radar TX in 28nm CMOS”; Giannini, et al.

After developing a matching receiver function (by end 2014), imec aims at building a complete multi-antenna lab prototype by the end of 2015. Then, integration of ADCs and digital logic will lead to a full SoC: the sought-after radar-on-a-chip.

Imec;
www.imec.be

www.edn-europe.com
Monitor multiple instruments, exchange data, on a single PC screen

Agilent’s BenchVue is a free-of-charge software tool that brings together the front-panel display information from multiple bench instruments, giving multiple-instrument measurement visibility on a PC monitor. Users will see accelerated testing, Agilent says, and you can capture and export measurement data and screen shots, and exchange data between instruments, with no programming necessary.

“Today’s bench-instrument users demand a faster, simpler way to accomplish their most common tasks,” said Rod Unverrich, senior program manager at Agilent. “BenchVue makes this possible with its simple point-and-click and capture operation, without the need to program. An integrated library feature further enables users to reduce test setup time through quick access to helpful manuals, FAQs and videos.”

BenchVue is intended to improve the way users interact with their instruments and the entire bench. Mobile apps let users monitor and respond to long-running tests from anywhere. BenchVue’s features include:

- Data logging and strip charts for digital multimeters and power supplies;
- Screen capture with annotation and trace data with preview charts for oscilloscopes and spectrum analysers;
- Waveform select and output control for function generators;
- The ability to control and share data across product families and even drag and drop waveforms between an oscilloscope and function generator; and
- No programming or instrument drivers required.

Compared to alternative software linking test and measurement instrument data to PC applications, Agilent says that BenchVue provides easier viewing, capturing and exporting of data and screen shots. The list of currently-supported Agilent instruments for BenchVue is here Download benchVue software for the PC free of charge; www.agilent.com/find/benchvue

ARM mbed + Arduino + STM32 MCUs in extensible development platform

A series of low-cost STM32 Nucleo prototyping/development boards deliver a combination of ARM Cortex-M-based microcontroller development boards, on an mbed platform, that add extensibility by providing headers for Arduino shields and direct connectivity to microcontroller peripherals. As an mbed-enabled board, developers can make use of the mbed open source software platform, online tools and collaboration infrastructure at mbed.org. The board’s Arduino headers accept shields from the Arduino ecosystem, allowing developers to add specialised functionality. ST will also offer its own dedicated shields supporting functions such as Bluetooth LE or Wi-Fi connectivity, GPS, audio recording (exploiting the company’s MEMS microphone expertise), proximity sensing, and wireless control.

Full STM32 Nucleo support for the STM32 family allows agile development with fine-tuning of both hardware and software on-the-fly at each prototyping stage. Investment in application shields is also protected, as any shield can be re-used with any STM32 Nucleo board and across various projects. The first four STM32 Nucleo boards support the STM32 F1, L1, F4, and F0 Value lines; further introductions will add support for the STM32 F3, L0, and F0 lines in Q2 2014. The STM32 Nucleo-F030R8, STM32 Nucleo-F103RB, STM32 Nucleo-F401RE and STM32 Nucleo-L152RE are priced from $10.32 per unit. The STM32 Nucleo-F072RB, STM32 Nucleo-F302R8, STM32 Nucleo-F334R8, and STM32 Nucleo-L053R8 boards will be introduced during Q2 2014. More details at www.st.com/stm32nucleo-pr
**Graphical environment to code middleware for ARM/STM32 MCUs**

In a second announcement around the STM32 line of ARM processors, ST has introduced STM32Cube, a software framework that uses a graphical configuration environment to simplify development. A full set of drivers over the entire STM32 product lines ensures easy porting among the different MCUs.

The STM32Cube software platform comprising tools, middleware, and Hardware Abstraction Layer allows you to focus on product-specific features; the first release of series-specific middleware, STM32CubeF4, supports the high-performance STM32 F4 series; support for remaining STM32 series will be added throughout 2014. A graphical configuration tool creates the initial customer source code, based on the combination of the microcontroller feature set and the STM32Cube drivers.

The development platform comprises the STM32CubeMX graphical configurator and initialisation C-code generator that provides step-by-step guidance for users and a set of rich embedded-software components that save integrating software from multiple sources. The software includes a new Hardware Abstraction Layer (HAL) that simplifies porting from one STM32 device to another. By gathering all the generic software components needed for developing applications on STM32 microcontrollers into one single package, this platform eliminates the complex task of assessing dependencies between individual software components.

The STM32CubeMX graphical configuration tool simplifies and automates configuration and generation of STM32 initialisation C code ready to be used with several development environments. STM32CubeMX is also available as an Eclipse plug-in, allowing use within Eclipse-based development environments. The tool provides a filter for selecting the desired STM32 device and graphical wizards to simplify configuration: the pin-out wizard assists pin assignment to avoid conflicts, embedding a powerful constraints solver; the clock-tree wizard assigns clocks and performs dynamic validation; the peripherals-and-middleware wizard aids configuration to avoid unusable settings; and the power-consumption wizard checks that the application meets the available power budget.

The new HAL, part of the STM32CubeF4 embedded software, offers a high abstraction level, simplifying the porting of an application from one STM32 microcontroller to another. The STM32CubeF4 middleware, includes a TCP/IP stack, a full USB Host and Device stack supporting multiple classes, the STemWin professional graphics stack developed by ST with SEGGER, the FatFS open-source file system, and the FreeRTOS open-source real-time operating system, coming with optional CMSIS-RTOS programming interface. The middleware components have simple license terms, either as open-source software or software delivered and supported by ST.

**mm-wave 256-QAM modem implemented as IP in FPGA**

Xilinx has announced a 1.6 Gbps low power, low cost, small cell backhaul modem, in the form of SmartCORE IP for millimetre wave applications; the 256 QAM modem supports both point to point as well as point to multipoint line-of-sight communications, addressing both 60-GHz and 80-GHz markets.

Added to Xilinx’ SmartCORE IP portfolio, this solution consumes less than 5W at data rates of over 1 Gbps. TDD multiplexing support is an additional feature which allows this IP to scale well from small footprint, low power, to high throughput wideband configurations.

“The [in the LTE market] we are in a period of unprecedented data growth, where wireless backhaul has a prominent role,” said Tarmo Pihl, wireless marketing director for Xilinx. “The 256 QAM millimeter wave modem IP will scale from 1+Gbps data rates today, to 10 Gbps in the future, and is designed to support the major shift and growth in mobile broadband traffic.” The highly configurable point-to-point and point-to-multipoint millimeter wave modem IP core incorporates all the key features and capabilities to accelerate development of next-generation wireless solutions. Suitable for outdoor deployment, the modem IP offers a highly scalable solution from low power small cell backhaul to high throughput wireless front haul applications using a common platform. It also supports several IP configurations such as a modem with either RS FEC or LDPC FEC, CPRI for fronthaul or 10GbE interface for backhaul, and JESD204B for a new generation of converter devices. The modem supports hitless and errorless adaptive modulation, analogue imperfection compensation, TDD and FDD multiplexing technologies with higher layer protocol interface, and granular channel bandwidths. The low DSP latency makes it suitable for wireless fronthaul applications with very stringent latency requirements.


www.edn-europe.com
TC3128 is a high efficiency, input current-limited buck-boost supercapacitor charger with active charge balancing for 1 or 2 series supercapacitors. It has an average input current limit that can be programmed up to 3A with ±2% accuracy, preventing power source overload while minimising capacitor recharge time. Efficient active charge balancing removes the need to balance inter-cell charging by dissipating power in ballast resistors, ensuring balanced operation and charging with mismatched capacitors, and less frequent recharge cycles.

A programmable maximum capacitor voltage clamp actively monitors and enforces the voltage across each capacitor in the series stack, ensuring reliable operation as capacitors age and develop mismatched capacities. The low noise buck-boost topology allows the output supercapacitor to be charged whether above or below the input. The low-RDS(on), low gate charge synchronous switches provide high efficiency conversion to minimise the charging time of storage elements. This combination of features makes the LTC3128 suitable for safely charging and protecting large capacitors in backup power applications.

The LTC3128’s input current limit and maximum capacitor voltage are each programmed using a single resistor. Average input current is accurately controlled over a 0.5A to 3A programming range, and the individual maximum capacitor voltage can be set from 1.6V to 3.0V. The input voltage range is 1.72V to 5.5V and the output voltage range, 1.8V to 5.5V. Other features of the LTC3128 include less-than 1μA quiescent current from VOUT in Burst Mode operation, accurate power-good and power-failure indicators, and thermal overload protection. Efficiency of charge transferred to the supercap is up to 96%.

The device comes in a thermally-enhanced 4 x 5 mm QFN and 24-lead TSSOP packages, both featuring operation from -40 to 125°C, for $3.95 (1,000).


USB, PC-hosted scope offers eight high-resolution channels and an ARB

An 8-channel PC oscilloscope from Pico Technology has 20-MHz bandwidth; housed in a similar style to Pico’s existing scope ranges, PicoScope 4824 offers 12-bit resolution, SuperSpeed USB 3.0 interface, and an integrated 14-bit arbitrary waveform generator (AWG).

The 8-channel PicoScope has the same small footprint as Pico’s existing 2 and 4-channel models, and according to its designers “can replace the cumbersome full-sized scope on your workbench”. It is entirely powered via USB and does not require a separate adaptor.

With 8 high-precision, low-noise inputs, a bandwidth of 20 MHz and sensitivity from 2 mV/div, this scope is aimed at a broad range of applications such as power supply start sequencing, decode and time-aligned display of related I/O, 7-channel audio, 3-phase voltage and current measurements, and multi-phase motor drives. The maximum sampling rate of 80 Msamples/sec, deep buffer memory of 256 Msamples and data streaming enable the scope to capture detailed timing data over prolonged periods.

The PicoScope 4824 includes a comprehensive list of features as standard, such as a 20 MHz FFT spectrum analyser, segmented memory (for bursts of up to 10,000 captures in less than 30 msec), math channels, automatic measurements, colour persistence display mode, advanced digital triggering, mask limit testing and serial decoding (SPI, I2C, I2S, RS-232/UART, CAN, LIN and FlexRay). A free SDK is also included for developing applications in various programming languages including C, Microsoft Visual Basic, National Instruments LabVIEW and MathWorks MATLAB with example code available at www.picapps.com

The PicoScope 4824 oscilloscope is available now from Pico distributors and from www.picotech.com, priced at €1688/£1395; this includes all of the features mentioned, plus USB 2.0 and USB 3.0 cables and a 5 year warranty.
Tektronix’ MDO3000 series of oscilloscopes are not just scopes; Tek refers to this range as six instruments in one, the six being scope, spectrum analyser, logic analyser, protocol analyser, arbitrary function generator and DVM.

Instruments that are extensible – in terms of their feature set – and upgradeable, in parametric terms, are popular: as the manufacturers’ documentation says, you are protecting your investment by not having to purchase a new unit when you move your own technology on. As more and more of the features of T&M instrumentation has come to be defined in software, it has also become common that the instrument you buy is capable, and fully-equipped, to operate at a higher specification than the one you initially purchase. A software key, that you subsequently purchase, enables more advanced performance than you bought at the outset. This benefits the manufacturers, who can limit the number of variants that they build (and they lock you in as a customer); and it means that your instrument is not obsoleted quickly, and does not have to return to its maker to receive an upgrade. It also enables the T&M vendor to offer you an “entry-point” specification – as distinct from an entry-point instrument – at a price that may fall into a lower capital-expenditure category.

Tektronix has applied all of these marketing strategies to its new MDO3000 series of oscilloscopes – or, not just scopes, as Tek refers to this range as six instruments in one, the six being scope, spectrum analyser, logic analyser, protocol analyser, arbitrary function generator and DVM. The spectrum analyser function follows the pattern that Tek set with the MDO4000 series in that it is a separate full-function channel, and not an FFT-derived analysis function applied to the main oscilloscope inputs.

By applying the expansion options approach outlined above, Tek offers an entry point that starts at €2,700/£2,250, and you get a spectrum analysis function to match the scope bandwidth you initially order; Tek says its customer research shows that over 25% of oscilloscope users now use a spectrum analyser multiple times per week – and that over 40% of embedded design projects include some form of wireless capability. EMI test is a major use of the spectrum analysis function.

The 3000 instrument “platform” can be upgraded in the field. Performance upgrades include analogue bandwidth of the oscilloscope and input frequency span of the spectrum analyzer. Functional upgrades include the addition of digital channels, protocol analysis, arbitrary function generation or digital voltmeter measurements. Bandwidth upgrades, for both scope and spectrum analyser, are tied to the specific serial number of the instrument – although you enable the upgrade by software key, Tek will send you a new front-panel label in the mail.

The MDO3000 Series oscilloscopes feature 2 or 4 analogue input channels with bandwidth ranging from 100 MHz to 1 GHz, 16 digital channels (optional) and one RF input channel matching the bandwidth of the oscilloscope (9 kHz up to analogue bandwidth). The RF input frequency on any model can be extended to 3 GHz. A “FastAcq” feature enables the MDO3000 oscilloscopes to run at more than 280,000 waveforms per second capture rate displayed on a digital phosphor display for easily finding infrequent anomalies in a signal. The integrated, optional 50 MHz AFG functionality is more than twice as fast as competitive offerings, Tek says, with eight times the arbitrary waveform record length.

MDO3000s also get 3.9 pF passive voltage probing on instruments with a starting price of €2,700/£2,250. For higher speed applications, 1 GHz (3-dB bandwidth) passive voltage probes are offered standard with 1 GHz instruments. 12-20 pF has been more typical of existing passive probes, Tek says.

There are ten pre-configured model options, 2 or 4 channels at 100, 200, 350, and 500 MHz, and 1 GHz, bandwidth. All use the 2.5 Gsamples/sec ADCs that Tek developed for existing scopes, that can be interleaved to 5 Gsamples/sec. A 2-channel, 100-MHz unit costs €2,700; a 4-ch 1GHz scope is around €11,200. Expanding the spectrum analyser from as-purchased bandwidth to 3 GHz costs $2500; the 16-ch digital input costs $1500, and the ARB, $750. And so on, through an extensive menu of retrofit options – for example, each serial protocol you need will add €908. For longer version of this article, click the link.
Developing IoT products is still much too complex, says Silicon Labs

The main components of an internet-of-things application have been available for some time: why have the numbers of such devices not yet taken off? According to Silicon Labs’ Geir Forre, senior vice president and general manager of MCU and wireless products, one reason is that development has been too complex. Forre commented to EDN Europe that if the expected billions of devices are to be realised, the development process must be made accessible to a wider user base. One step along that road is the company’s free-to-download Simplicity Studio Platform, a design environment that provides unified support for 32-bit EFM32 Gecko microcontrollers (MCUs) and 8-bit MCUs. The new Simplicity Studio platform also integrates an Eclipse-based integrated development environment (IDE) that supports both 32-bit and 8-bit embedded designs.

Simplicity Studio is designed to give embedded designers using Silabs devices with everything they need to complete their projects, from initial concept to final product. The platform has built-in intelligence to detect the connected target MCU. Graphical hardware configuration tools automatically configure the MCU, freeing the developer from studying technical documentation. Developers can get projects up and running in minutes with sample demos and application code examples.

Embedded developers can use the integrated Simplicity IDE to develop and debug their firmware. The IDE supports Eclipse plugins, uses the Eclipse Debugger for C/C++, and supports Keil and Gnu Compiler Collection (GCC) build tools. Silicon Labs also provides 8-bit MCU developers with Keil PK51 build tools at no charge. For customers who prefer the Keil μVision or IAR Embedded Workbench IDE, there is third-party tools support, allowing developers to launch their preferred IDE from inside Simplicity Studio. The package also configures MCU pin-out and peripheral placement and generates the relevant C-code. The configuration tools also automatically resolve pin-out conflicts.

The real-time energy profiling and analysis tools for estimating power consumption and balancing performance and energy efficiency, that already exist for the Gecko MCUs, are included. The energyAware Battery Calculator helps developers estimate current consumption and battery life. Developers can select EFM32 MCU Energy Modes and battery configuration and estimate power consumption before writing any code. The energyAware Profiler analyses current consumption in real-time, identifying areas of code that should be optimised if current draw is too high. Users can access demos, software examples, data sheets, application notes, technical support and community fora. Forre calls it, “…a major leap forward in productivity.”

Add safety-critical features to control applications with 8-bit PICs

Microchip has added low pin-count, general-purpose 8-bit PIC MCUs that have features addressing safety-critical applications: a 24-bit Signal Measurement Timer (SMT) enables more precise and accurate measurements, and these PICs gain hardware Zero Cross Detect (ZCD) for robust operation, plus fault-detecting hardware including a Hardware Limit Timer.

Low pin-count PIC16(L)F161X devices add to Microchip’s Core Independent Peripherals (CIP), which off-load timing-critical and core-intensive tasks from the CPU. These devices integrate fault-detecting hardware features for safety-critical applications. The Windowed Watchdog Timer (WWDT) monitors proper software operation within predefined limits. The Cyclic Redundancy Check with Memory Scan (CRC/SCAN) detects and scans memory for corrupted data. This family also includes a Hardware Limit Timer (HLT), which detects hardware fault conditions, including stall and stop, to simplify closed-loop-control applications. These peripherals make it easier for designers to implement safety standards such as UL & class B, or fail-safe operation.

Microchip asserts that coding and additional hardware associated with implementing safety in an embedded system can be reduced by exploiting these integrated hardware features. PIC12(L)F1612 MCUs come in 8-pin PDIP, SOIC, and 3 x 3 mm DFN and UDFN packages. The PIC16(L)F1613 MCUs come in 14-pin PDIP, SOIC, TSSOP, and 4 x 4 mm UQFN and QFN packages. More at; www.microchip.com/get/VDLM

Also added by Microchip, and relevant to control and automation designs, are 8-bit PICs with three high-resolution 16-bit PWMs, in 8-pin packages. PIC12(L)F157X family chips have multiple 16-bit PWMs with an assortment of analogue peripheral and serial communications in an 8-pin package. These MCUs deliver three full-featured 16-bit PWMs with independent timers, for applications where high resolution is needed, such as LED lighting, stepper motors, battery charging and other general-purpose applications. In addition to standard and centre-aligned PWM output modes, the peripheral also has four compare modes and can serve as an additional 16-bit timer.

The PIC12F1572 enables communication with an EUSART, enabling general-purpose serial communication and LIN for automotive and industrial control. The integrated 10-bit ADCs enable human-interface/touch applications using Microchip’s capacitive mTouch sensing solution. Additionally, the chips offer non-volatile data storage via High Endurance Flash (HEF) memory. The “LF” versions feature low-power technology, for active currents of less than 35 µA/MHz and sleep currents down to 20 nA, which is ideal for battery-powered applications. Microchip; www.microchip.com/get/G6RB

For a longer version of this article, click the link.
Digital video transmission rates have steadily increased since the introduction of high-definition video. The latest trend in the industry for high-resolution video is the market adoption of 6G-SDI to support 4K digital cinema and ultra-high definition (UHD) television. Digital video data delivery at higher speeds required by 6G-SDI poses new challenges in designing broadcast video production and transmission equipment.

In particular, high frequency, low-jitter clocking solutions are a critical element to maintain proper signal integrity through the various components and interconnecting cables that constitute the high-definition video network. In addition, these timing solutions must be flexible enough to accommodate the multiple frequencies required by legacy video standards.

Higher-speed video standards on the horizon

The Society of Motion Picture and Television Engineers (SMPTE) was founded in 1916 to standardise video content distribution. Video equipment manufacturers have since adhered to these standards. In 1997, the SMPTE established the SD-SDI 259M standard, which was the first ratified definition of a serial digital interface (SDI) to send and receive uncompressed digital video over 75-Ohm coaxial cable within a studio environment. SDI supports transmission rates ranging from 270 Mbps to 360 Mbps.

Due to the fact that digitised video signals accumulate jitter across video components and interconnecting cables, SMPTE established limits on the allowable jitter content of SDI signals. As high-definition digital video advanced to 720p and 1080i, SMPTE defined the HD-SDi 292M standard to support higher bandwidth video transmission at 1.485 Gbit/sec.

In 2005, the SMPTE introduced 3G-SDI to enable the transmission of 1080p video at 2.97 Gbps over existing 75-Ohm coaxial cable. To support these higher video transmission speeds, the SMPTE has set increasingly stringent jitter requirements. Table 1 summarises the timing requirements for the SMPTE-ratified SDI standards.

In recent years, continued technological innovation in digital video has pushed the boundaries of video resolution from 1080p (2K resolution) to 4K. Transmitting a larger number of pixels on the same infrastructure implies having to deliver the video payload at 5.97 Gbit/sec. The goal of the standards published by the SMPTE has been to guide the increasing data transmission rates to ensure that existing video production facility infrastructure can support and broadcast higher resolution video. Although the SMPTE body has yet to ratify a standard for 6G-SDI, video equipment suppliers are already meeting the demand for 4K by introducing solutions to support the faster data rates.

Early 6G/12G-SDI market adoption

In response to surging interest and demand for 4K video components, broadcast video equipment suppliers are starting to release 6G-SDI compatible products such as 4K production switches, video routers, encoders/decoders, video monitors, video servers and video converters. In addition to enabling transmission of UHD video over standard BNC cable, this equipment supports simplified switching between UHD, HD and SD formats.

This enables broadcast video engineers to easily switch between different formats depending on their content production requirements. This flexibility eases the migration to UHD by enabling studios to leverage their existing investment in HD and SD equipment and continue to produce content in a variety of formats.

Semiconductor manufacturers have followed suit and have started to release ICs that are purpose-built for 6G-SDI. These devices include cable equalisers, cable drivers, reclockers and FPGAs with integrated SDI transceivers. One limitation with 6G-SDI is that 4K UHD can be transmitted at no more than 30 frames per second. Higher data rates are required to transmit video at higher frame rates. Anticipating this demand, manufacturers are starting to release 12G-SDI components that support data rates of 11.8 Gbit/sec.

Taking these “proprietary” solutions to available-product status [in the absence of, or in anticipation of, relevant standards] increases the risk of future interoperability concerns. For this reason, the SMPTE has assembled a new Working Group to define UHD single-link, dual-link and quad-link electrical and optical SDI interfaces with nominal link rates of 6 Gbit/sec, 12 Gbit/sec and 24 Gbit/sec to support next-generation multimedia, high-frame-rate data transmission.

In the continuation of this article, the authors continue with a discussion of three key timing-related design challenges affecting 6G-SDI applications.
H-bridge: black box or are details important?  By Kevin Craig

Engineers in all disciplines use electronics in their designs for sensing, actuation, and real-time control. Today there are few exceptions. A common component is an operational amplifier (op-amp), which most engineers treat as a black box containing many transistors and resistors. Its performance is primarily determined by the components (e.g., resistors and capacitors) surrounding it as long as the op-amp has negative feedback and its limitations are not exceeded.

Another common electronic component is the H-bridge. Any engineer who has ever controlled a motor has most likely used the H-bridge, but perhaps treated it as a black box with no thought as to how it works and how it affects overall system performance. The H-bridge needs to be thoroughly understood for model-based design and optimum system performance.

The H-bridge, as shown in the diagram, is named because of its configuration. It has four power devices (transistors, MOSFETs, are typical, p-channel for the high side and n-channel for the low side in the diagram) with the load (usually brushed dc or stepper motor) at the centre. The diodes are of the Schottky type with short turn-on delay. The four transistors can be turned on and off independently. If transistors 2 and 3 are turned on, the motor turns in one direction; turn transistors 1 and 4 on and the motor turns in the opposite direction. The transistors are usually controlled in a pulse-width modulated (PWM) fashion. When the transistor is on, it behaves like a small temperature-dependent resistor, the lower the value the better for heat dissipation.

When the transistor is completely off, it conducts no current. MOSFETs are voltage-driven devices; the gate forms a parasitic capacitor with the source, and this capacitance limits the speed at which the transistor can be turned on and off. In the transitional periods, the power dissipation due to switching is significant, especially when the switching frequency is higher than a few hundred Hz. The role of the diodes is often overlooked. While the bridge is on, two of the four transistors carry the current and the diodes have no role.

However, when the load is inductive, as with motors, and the bridge is commanded to turn the load off, the electromagnetic field associated with it will collapse and the stored energy will start to dissipate either through the bottom transistors and diodes or through the top transistors and diodes. The dissipated heat from the diodes can be of the same order of magnitude as the heat dissipation from the transistor switching.

The load (motor) is modelled as an inductor ($L_m$), resistance ($R_m$), and speed-dependent voltage (back emf) in series. The motor torque depends on the current flowing through this series combination. There are two extremes. When the motor runs with no load, the current is low and the motor terminal voltage is close to the back-emf voltage. When the motor is stalled, the back-emf voltage is zero and the motor acts like an inductor.

The H-bridge can be driven in many different ways. In general, the on-time behaviour is rather simple: turn on one high-side transistor and the opposite low-side transistor to allow current to flow through the motor. It is the off-time drive that makes the difference. Since transistors 1 and 2 (or 3 and 4) should never be turned on at the same time, there are only three different combinations for those two switches: transistor 1 conducts, or transistor 2 conducts, or neither conducts. There are many different drive modes. András Tantos has provided an excellent, detailed explanation here. I highly recommend it.

The understanding of the internal behaviour of the H-Bridge is of fundamental importance for motor control system design and also to mitigate electromagnetic effects while controlling inductive loads, which can affect the performance and behaviour of surrounding circuits.
TE networks and signals present a range of problems for the RF front end in handsets as the signal characteristics differ greatly from previous 2G and 3G standards. Key metrics such as battery life, antenna performance, network coverage and thermal management are negatively affected by issues in the RF front end. Central to these challenges is the RF power amplifier (PA), its performance and power consumption.

Envelope Tracking (ET) is a new power modulation technique being used to optimise the performance and efficiency of the PA to help overcome the technical challenges presented by complex LTE signals. Indeed ET has largely been accepted by mobile handset manufacturers as the de facto standard RF PA power supply modulation architecture for LTE phones due to enter the market in 2014.

Alongside ET, some chipset companies are looking at a signal processing technique, Digital PreDistortion (DPD), as a way to optimise PA performance. Although many assume the two techniques perform similar tasks, it is important to clarify that DPD offers no efficiency benefits. DPD is a linearisation technique, and so ET and DPD are performing different functions in RF front end design. It is possible to use both techniques in isolation or together.

However, DPD is not an easy technology to develop. For designers there are important questions to resolve, such as: how do ET and DPD interact? How do I implement them in isolation? How do I use them together? If I have ET, do I need DPD, and vice versa?

As a result we have seen several different approaches from LTE chipset vendors. Some are not implementing DPD at all, some have implemented DPD but are not yet using it, others are using ET on its own and some are using DPD in conjunction with ET. Why is this? What might this split in approaches mean for the industry? This article looks at the technical advantages and disadvantages of DPD in the RF front end of handsets, the wider implications of vendors choosing the DPD route or not, and how DPD and ET can be used together most effectively.

**Efficiency vs linearity**

ET is a very fast power supply modulation technique that improves the energy efficiency of RF power amplifiers (PAs). It replaces the traditional fixed DC supply voltage to the RF PA with a dynamic supply voltage, which closely tracks the instantaneous amplitude, or "envelope" of the transmitted RF signal (See Figure 1).

RF PAs in handsets are typically operated in a classic Class AB configuration, and are only at their most efficient when the RF envelope waveform is close to peak power. This is not a problem with such traditional signals as 2G GSM, where information is encoded only in the phase of the signal - the amplitude is constant, and the PA can operate in this high efficiency mode all the time. GSM PAs consequently have typical efficiencies of 50-55%. However, as data rates increase from 2G to 3G and 4G, the increased spectral efficiency forces information to be encoded in the amplitude, as well as the phase, of the signal. When amplifying RF signals with high crest factors such as 4G LTE waveforms, the average efficiency of the PA drops significantly, with figures of 20-25% being common.

Modulating the supply voltage dynamically, in synchronisation with the envelope of the transmitted RF signal, ensures that the output device stays in saturation – its most efficient operating region – for a large portion of time, by providing just the minimum instantaneous supply voltage to the PA on a sample-by-sample basis. This can restore the PA efficiency to 50-55%, even for high crest factor 4G signals, offering the promise of 4G performance with 2G battery life.

This efficiency gain is a major benefit for product designers. However, if an ET PA is operated in maximum efficiency mode, then it will introduce distortion that compromises the linearity of the PA. So although you may be achieving maximum PA efficiency, some form of linearisation will be needed to correct this distortion (See Figure 2).

In the continuation of this article, the author considers the distinct contributions of ET and DPD, and how they can be used together or separately.
OVERCOME THE CHALLENGES OF DRIVING PARALLEL LED STRINGS

LEDs are finding their way into more products than ever before. Automotive lighting, TV backlights and tablets are just a few applications that require multiple LEDs. Driving a large number of LEDs with a constant current can be done with either a lengthy series connection or by driving multiple strings in parallel. But connecting many LEDs in a long series string poses high-voltage and single-point failure issues. Similarly, powering multiple strings in parallel requires multiple current regulators, one for each string. Ultimately, this leads to higher complexity and cost. Today’s trend is to operate strings in parallel, and this article explores options and the rationale for implementing circuitry to achieve this goal.

An LED is similar to a standard diode by virtue of being a current-driven device. It has an I-V curve in which the current and voltage are non-linear and a small change in its forward voltage can translate into a large current change. Since the LED current in nearly proportional to the LED’s luminous flux, it is important in applications such as TVs to control the current accurately. But not all applications necessarily require high accuracy for brightness matching of the LEDs. If the LEDs are driven in a single string, there is inherent matching because each LED has the same current level. As the number of LEDs in use increases, paralleling strings becomes necessary, and a choice must be made as to how to control the current in each string.

A typical white LED can have a forward voltage of 3.3V with as much as a 20% variation at its rated current. If 10 LEDs are used in series, it’s possible that one string may require 33V to adequately drive it, while a second string requires 39.6V at the same current. If these two strings are wired in parallel, the lower voltage string pulls significantly more current than intended and the second significantly less. The probability that all the LEDs in one string would fail at the high end of its forward voltage specification is rather small and this probability decreases as more LEDs are used.

In reality, balancing between these two strings is much better, but there could still be a difference of several volts. To help this situation, LED manufacturers use binning to sort parts into groups that accurately match the LEDs forward voltage (Vf) drops (as well as flux and wavelength) to allow better performance. Figure 1A shows a simple, low-cost implementation for paralleling two strings. A fixed-voltage source and a simple resistor to set the current level is all that is necessary.

The voltage across one sense resistor can be regulated by an external control circuit to adjust the output voltage higher or lower to accurately control the LED current. While this regulates the LED current in one string, it does not necessarily do a good job for the second. It can actually make the current in the second worse, as in the case where the control loop increases the output voltage for the regulated string, but the second string has the lower voltage drop of the two.

As in standard diodes, the forward drop of LEDs decreases with increasing temperature. If one string gets significantly hotter than the other, its forward drop decreases and it begins to draw more current. This added dissipation heats it further, increasing its current and possibly leading to LED failure due to this thermal runaway. This situation requires that the voltage driving the strings is current regulated and is constant. Additionally, all LEDs should be mounted on a common heatsink to keep the operational temperature between them as equal as possible.

Thermal runaway isn’t a problem when the strings are driven by a constant voltage, but the current matching between strings can be quite poor. Since each string is independent of the other (that is, the current in one is not directly regulating the current in the other), fault tolerance is good when driven by a voltage source, but poor when current is regulated in one string (via Vfb). In this situation, if an LED opens in the regulated string, the voltage driving the strings is commanded higher by the control circuit and eventually causes overvoltage in the unregulated string, leading to failure. While adequate when driven by a voltage source without feedback, the circuit of Figure 1A doesn’t provide accurate current matching in the LED strings for more demanding applications.

Figure 1B implements a current mirror to regulate the currents in both strings. The first string uses voltage feedback (Vfb) from sense resistor Rs1 to regulate its current and relies on Vbe of Q1 and Q2 matching to set the same voltage across Rs2. With the same sense resistor voltage and value, the same current is forced to flow in the second string. The regulation accuracy largely depends on the matching between the Vbe voltages of Q1 and Q2. For this reason, a dual transistor with both components on the same die helps reduce temperature, processing and lot variations.

This article continues by outlining circuits that provide more accurate current control, and that accommodate the situation of driving strings of LEDs with unequal voltages.
THINKING ABOUT THE INTERNET OF THINGS (IoT)

What does the phrase “Internet of Things” mean? It depends a lot on where you stand in the supply chain. Many have tried to define it, and the definitions are often coloured by the needs of their own industries and their own agendas. But, as a hardware or software engineer, you already understand the essential element: to build products that are interconnected. And, embedded systems will play – and are playing – a crucial role in the development of the IoT.

From what I see today, there are four main components of systems that support the Internet of Things, as depicted in Figure 1.

As you see, there are four separate areas:
- The Thing itself (the device)
- The Local network, which moves data in and out of the device. This may include a gateway to translate proprietary communication protocols to the IP family of protocols.
- The Internet itself
- End user devices (desktop, laptop, smartphones) or enterprise data systems that receive and manipulate data (backend data analytics)

IoT is not complicated in conception, but it is complex in its execution. Each individual component is simple, but there are many required components for IoT. What is important to understand is that even if new hardware and software are still under development, we already have all the tools we need now to start making IoT a reality.

This article will look at the end devices in an IoT system from the embedded developer point of view. This article has four parts, divided along the same grouping found in Figure 1. I would like to start with the “Thing”. But to understand well the “Thing” challenges, we need to understand the communication technologies in play with the IoT devices.

WHAT ARE THE LOCAL NETWORKS?

As mentioned above, the value in IoT is in interconnected devices, and the data and metadata they will generate. The choice of communication technology affects the amount of software required, which in turn affects hardware requirements and cost. Furthermore, IoT devices are deployed in such a huge number of different ways—in clothing, houses, buildings, campuses, factories, and even in your body—that no single networking technology can fit all bills.

WIRELESS SENSOR NETWORKS (WSN)

For an installation of IoT devices in a specific location (say, a factory), a large number of sensors and actuators may be scattered over a wide area. A wireless technology is the best fit for such devices. There are as many types of edge/sensing node as there are system types, and some of these systems already have associated standards. This is why there are so many machine-to-machine (M2M) communication technologies in use. Some of these technologies pre-date the concepts of IoT and M2M, and they all have their particularities in terms of radio frequency, power consumption or protocol complexity. So, choosing a local networking technology can be a serious problem for embedded developers. There is often no single best choice. The technologies currently available are narrowly specialised for specific vertical markets (smart healthcare, smart grid, and so on).

Figure 2 shows the position of the nodes and edge nodes in a Wireless Sensor Network. A description of these devices follows in the continuation of the article; click on the link, right.
Measuring amplifier DC offset voltage, PSRR, CMRR, and open-loop gain

Operational amplifier (op amp) offset voltage is an important parameter to understand. It is a voltage error that is a consequence of the op amp’s mismatched input stage (Figure 1).

The offset error appears as a DC voltage at the output pin (V\text{OUT}, Figure 2). The offset-voltage (V_{OS}) is gained from the relationship, \( G = (1 + R2 / R1) \); This is the same as a voltage source connected to the amplifier’s non-inverting input (IN+) of your amplifier. If you have a high closed-loop gain around the amplifier, the offset voltage appears as a significant voltage error in any precision circuit that you may implement. But, the consequence of this error goes much deeper than simply an output offset voltage. Its level may shift the results of some of the amplifier’s other important parameters: the power-supply-rejection-ratio (PSRR), the amplifier’s common-mode-rejection-ratio (CMRR), and the open-loop-gain (A_{OL}) specifications.

You can measure the PSRR by changing the power supply voltages and noting how the voltage offset changes. The amplifier CMRR is measured by observing how the voltage offset changes as the input common-mode voltage at the amplifier’s input stage changes. Finally, \( A_{OL} \) is measured by observing \( V_{OS} \) changes as \( V_{OUT} \) changes.

Figure 2 shows a simple circuit diagram that you can use when measuring these specifications at DC. In this circuit, \( V_{OS} \) is extracted at the VX node. From the VX value you can calculate the offset voltage (\( V_{OS} \)). It is equal to, \( V_{OS} = V \times R4 / (R3+R4) \).

For the PSRR specification the applicable formula is:

\[
PSRR(dB) = 20 \times \log \left( \frac{V_{OS}^+}{V_{OS}^-} \right) \quad \text{V}_{OS}^+ \quad \text{V}_{OS}^-
\]

Where PSRR is equal to the power-supply-rejection-ratio specified in dB, \( V_+ \) is the positive voltage supply \( V_- \) is the negative voltage supply and \( V_{OS} \) is the measured operational amplifier offset voltage.

Referring to Figure 2, one measures \( V_{OS} \) for two power supply settings. As you change the power supply voltages, be careful to stay within the amplifier’s operating specifications. During this test, the input common-mode-voltage (CMV), or V1, and the amplifier’s \( V_{OUT} \) remain set to the mid-supply level. If the output does not remain at that level, you can manipulate this voltage by adjusting \( V2 \). Similar techniques are used to measure the CMRR of an amplifier. Changing the input CMV (V1) causes \( V_{OS} \) to change. The formula for CMRR is:

\[
CMRR(dB) = 20 \times \log \left( \frac{V_{1,1}}{V_{1,2}} \right) \quad \text{V}_{1,1} \quad \text{V}_{1,2}
\]

Where CMRR is equal to the common-mode-rejection-ratio in dB: \( V1-1 \) is the first common-mode voltage setting \( V1-2 \) is the second common-mode voltage setting \( V_{OS} \) is the measured operational amplifier offset voltage.

Again, it is important to make sure that the output voltage remains halfway between the two power supply voltages. This can be accomplished by adjusting \( V2 \). Also, the power supplies remain constant. Additionally, be careful to keep the non-inverting input pin (V1) within the product data sheet’s limits. The final DC test is open-loop-gain (\( A_{OL} \)). \( A_{OL} \) is equal to changes in the output voltage with respect to changes in the offset voltage. You can change the output voltage by changing the voltage at the \( V2 \) node in Figure 2. The formula for \( A_{OL} \) is:

\[
A_{OL}(dB) = 20 \times \log \left( \frac{V_{OS}^1}{V_{OS}^2} \right) \quad \text{V}_{OS}^1 \quad \text{V}_{OS}^2
\]

Where \( A_{OL} \) is equal to the amplifier’s open-loop-gain in dB:

\( V_{OUT} \) is the output voltage of the amplifier \( V_{OS} \) is the measured operational amplifier offset voltage In this case, it is important to make sure that the input common-mode voltage (V1) remains halfway between the power supply voltages, and that the power supplies are constant. Additionally, during this measurement the output voltage pin (\( V_{OUT} \)) must remain within the product data sheet’s specified limits. Table 1 summarises all of these test conditions. You can change the voltage of \( V2 \) to meet the conditions in Table 1. These are easy DC tests to run when you are trying to understand how the amplifier reacts to the different power supply, common-mode input voltage, and output voltage conditions. Give these tests a try on your favourite amplifier and compare your results to the respective product data sheet. I would like to know if you get your expected results.

References

“Will the real \( V_{OS} \) please stand up?,” Matthew Pickett, Analog Wire, Texas Instruments

“Will the real \( V_{OS} \) please stand up?,” Tim Green, Precision Designs Hub, Texas Instruments

“My amplifier has high PSRR, so I don’t need to worry about supply variation…Right?,” Art Kay, Precision Designs Hub, Texas Instruments

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Table 1 \( V_{OS} \), PSRR, CMRR, and \( A_{OL} \) test guidance for Figure 1 circuit.
widely used methodology for testing digital circuits is to add scan test structures to the design and then deliver test patterns through these structures that reveal defects when the chip responses are observed. The approach has been in use for decades and is based on modeling circuit defects to a level of abstraction that enables a computationally efficient test pattern generation process.

The simple stuck-at fault model was initially used and it modelled circuit defects as logic nets stuck at either a 0 or 1 value. More complex fault models were added over the years to account for new defect types that appeared as the industry transitioned to new technology nodes. Among the more recently adopted fault models were the transition, bridging, open and small-delay faults.

But with the move to smaller geometries, these fault models and associated test patterns are becoming less and less effective at ensuring desired quality levels. The main problem is that all of these existing fault models only consider faults on cell inputs and outputs and on interconnect lines between these cells. In other words, only faults abstracted to the netlist level are explicitly considered.

It turns out, however, that increasingly more defects occur within the cell structures. For the more advanced technology nodes and associated fabrication technologies, some estimates put the number of defects found within cells to represent almost half of all circuit defects. Thousands of patterns are typically produced during the normal ATPG (automatic test pattern generation) process. As a result, although traditional fault models do not target cell-internal defects, many of these defects end up being detected by chance.

However, when considering millions of gates in a design, relying on luck to detect potential defects within each cell is not a dependable strategy. One option would be to apply every possible combination of inputs at every gate. This fault model is referred to as the gate-exhaustive fault model. It would certainly be effective in detecting all static cell-internal defects since it would apply every possible combination.

For example, for an 8 input cell, gate-exhaustive testing would apply all possible \(2^8 = 256\) input combinations. It is easy to see that applying such an exhaustive set of patterns quickly becomes impractical. To make matters worse, many defects inside cells are timing-related and therefore are not detectable using static tests. A two-pattern test is necessary to detect such defects. So for the 8 input cell example, two-cycle gate exhaustive testing would require the application of \(2^8 \times 2^8 = 65,536\) patterns. For designs with very high quality requirements, a much more efficient test strategy for detecting cell-internal defects is clearly necessary.

Cell-Aware test is a transistor-level ATPG-based test methodology that achieves the needed efficiency improvements by directly targeting specific shorts, opens and transistor defects internal to each standard cell, resulting in significant reductions in defect (DPM) levels.

**CELL-AWARE TEST UPDATES ATPG METHODOLOGIES**

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**CELL-AWARE MODEL CREATION**

The Cell-Aware test approach starts with an automated cell library analysis process, which is illustrated in Figure 1. Each semiconductor process node has a set of technology cell libraries used to describe the logic behaviour and physical layout of the lowest-level component in the netlist. The Cell-Aware library analysis process begins with an extraction of the physical library, represented in GDSII. Each extracted cell results in a transistor-level netlist with parasitic resistances and capacitances. A resistance location represents a conductive path with the potential for an open defect, while a capacitance identifies locations with the potential for a bridge defect. Parasitics that lead to transistor open and drive-strength defects are also considered (a detailed discussion of these defects related to FinFET transistors is provided later).

An analogue simulator is then used to simulate each potential defect against an exhaustive set of stimuli to determine if there are sets of cell inputs that produce an output sufficiently different than the defect-free result.

Analogue simulations are performed with each parasitic capacitor replaced with a resistor of increasing resistance values (e.g. 1Ω, 10Ω, 100Ω, 500Ω, 1 kΩ, 5 kΩ, 10 kΩ, and 20 kΩ). Similarly, simulations are performed with each parasitic resistor replaced with a large (e.g. 1 GΩ) resistance. The input patterns and results of each simulation are compared to the good-circuit simulation results. Defects are categorised as detected when the cell’s output voltage deviates from the “good circuit” voltage by a specified percentage (typically 50%). Not all bridge or open defects are detected in the analogue fault simulations described above. This is due to some bridges causing a small-delay defect. A small delay defect only affects the circuit when it is operated at-speed. For these defects, 2-cycle analogue fault simulation is necessary.

The final step in cell-aware analysis process is to convert the list of input combinations into a set of the necessary input values for each fault within each cell. Because this information is defined at the cell inputs as logic values, it is basically a logic fault model representation of the analogue defect simulation. This set of stimuli for each cell represents the Cell-Aware fault model file for ATPG. Within this file, a simulated defect (now a fault) can have one or more input combinations. Note that because the Cell-Aware library analysis process is performed for all cells within a technology library, any design using that technology can read in the same Cell-Aware fault model file. Analysis only needs to occur once and then can be applied to any design on that technology node.

*The complete paper is available from the White Papers section of EDN Europe’s website; follow the link below.*
Medical-equipment designers can use high-performance FPGAs to boost performance while reducing power consumption, system cost, and development time.

Consumer electronics have taken great strides forward over the past decade in terms of affordability, size and power. In contrast, medical electronics has yet to experience a similar type of innovation. However, an increasing world population, longer life expectancy and rising standards of living should become catalysts for a medical devices revolution that will help improve general wellbeing while reducing healthcare costs.

The following are some key design challenges for medical electronics designers:

1. Features differentiation – Competition is increasing within medical electronics markets, as attractive margins drive various manufacturers to deliver products with differentiating features and advanced performance to stay ahead of other contenders.

2. Power reduction - There will be a tight power budget ahead for medical devices as future medical electronics prioritise wireless operation and focus on miniaturisation. Reducing power consumption can lead to better thermal management thus reducing overall product size.

3. Development time – Medical electronic devices must pass a lengthy certification process which can significantly slow down time to market. The typical development cycle for consumer electronics products is 3 to 9 months, whereas typical medical electronics average 2-3 years. Tools and methods available to reduce development time and aid in certification will be vital.

These challenges can cause engineers to make unwanted tradeoffs between features and cost, or power and size. The design of ultrasound equipment provides a prime example.

Ultrasound imaging

Due to its non-invasive nature, ultrasound imaging is used across many medical applications from diagnostic investigations to therapy. High-performance ultrasound machines offering the highest resolution and state of the art 4D image viewing are still cart-based and bulky. On the other hand, portable or handheld versions have significant limitations in terms of battery life and image quality. Clearly the performance-to-size ratio still needs to be improved. One could envision a future in which personal ultrasound machines could be marketed to expectant parents. For this to happen, however, the equipment would have to reach consumer-level pricing, portability and ease of use. We may be a few years away from realisation of such product, but what are the products and platforms that can help solve the design challenges of medical designers and improve the performance/size or performance/price ratio?

For many years Field Programmable Gate Arrays (FPGAs) have been central to the enablement of medical ultrasound technology. FPGAs have a long product life cycle which can match the long time-in-market requirement for medical electronics. Performance and flexibility are two primary attributes that make FPGAs the device of choice for ultrasound imaging. By allowing algorithms and features to be updated without needing to change-out components, FPGAs enable systems to become essentially future-proof. With every technology node shrink, FPGAs provide increased performance to price ratio; for example moving from 28nm to 20nm can result in 20-50% performance improvement while also reducing power consumption. In addition, FPGA tools support an abstracted design flow, performing automated timing closure and minimising place-and-route time, leading ultimately to shorter development time. By continuing to provide such advantages, FPGAs will remain critical to the design of next-generation ultrasound equipment.

Let’s explore how to satisfy the functional requirements of a medical ultrasound system. An ultrasound imaging system can be split into three main functions: front-end, transmission, and back-end. Programmable technology such as FPGAs plays a crucial role in each of these blocks.

The objective of an ultrasound front end is to control transmission of ultrasonic pulses and capture the reflected sound data. Analogue-to-Digital Converters (ADCs) convert the reflected ultrasonic data into digital format. Most of the ADCs used in ultrasound imaging applications support from four to eight channels and 12-16 bits resolution at 40-60 Msamples/sec. Cart-based ultrasounds require high resolution, often with as many as 128 or even 512 channels, whereas a portable ultrasound that must meet low weight and size targets may have as few as eight channels. In order to support the high volume of data transmission, ADC outputs typically use Low Voltage Differential Signalling (LVDS). Because an FPGA has a large number of input/output (IO) blocks which can be configured to support LVDS, it can aggregate data from several ADCs for preprocessing.

In the continuation of this article, the author cites the ability of FPGAs to handle fast data streams, as a further strength of the technology for medical system designs.
Safety flasher warns of high voltage

by Clive Bolton

Working on high voltage circuits can be dangerous. Capacitors can maintain high voltage in a system for a considerable time after power is removed.

Running an LED off a high voltage source typically means that significant power is dissipated in a current limiting resistor. Using a resistor means that the LED is bright when the circuit is at its full operating voltage, but dimmer as the voltage ramps down. Indeed, the LED may not provide much of a warning at voltages that are still considered unsafe.

This Design Idea uses a Linear Technology LTC1540CS8 combination nano-power comparator and reference to flash a high brightness LED when high voltage is present. The LED flashes rapidly at high voltages and slowly at lower voltages. Because the LED duty cycle is low, the current draw is also low. The high brightness LED draws attention even under well lit conditions.

C1 is charged through resistor ladder R1-R3. The voltage across C1 is scaled by resistor divider R4 and R7. The comparator compares this voltage against the 1.18V internal reference diode. R5 and small signal diode D1 provide hysteresis. With the values shown, the LED is turned on when the voltage across C1 is 5.5V, and turned off after the voltage decreases to 3.6V. The LED on-time is nominally 5msec.

At 210V, the LED flashes at 25 Hz and the circuit draws about 300 µA. At 100V, the LED flashes at 11 Hz, and the circuit draws about 100 µA. At 50V, the LED flashes about once per second, and the circuit draws 60 µA. In the prototype, the circuit was still flashing at 0.5 Hz after the input voltage had declined to a safe 20V.

The circuit can be modified to suit different requirements. Doubling the value of C1 halves the flashing rate. Increasing the value of resistor ladder R1-R3 allows the circuit to operate at higher voltages, albeit with a proportionally shifted lower operating voltage limit. With the values shown, the circuit works from under 20V to well over 500V. Note that the 0603 size resistors used for R1-R3 are only rated for 75V and additional series resistors may be necessary when operating at higher voltages. If a high voltage diode is added at the top of the ladder, the circuit will also work with AC voltages.

If a relatively constant flashing frequency is desirable, R1-R3 may be replaced by current source Q1-Q2. The values shown result in a much more limited 2 Hz to 1 Hz flashing range as the supply ramps down from 250V to 50V.

Optional Current Source (replaces R1-R3)
The TL431 is a three-terminal programmable shunt regulator that implements Zener-like references with low temperature coefficients. Its output can be programmed from the internally set reference of about 2.5V to 36V using two external resistors. In addition, it exhibits a wide operating current range of 1.0 mA to 100 mA with a typical dynamic impedance of 0.22Ω. The characteristics of these references make them excellent replacements for Zener diodes in many applications such as digital voltmeters, power supplies, and op-amp circuitry, where precision voltage references are needed. Today, they are ubiquitous in switching-mode power supplies.

The TL431 exhibits an interesting instability under certain conditions of input supply voltage and capacitive load, causing sustained oscillations that can range from 10 kHz up to 1.5 MHz, generally depending on the control input voltage. This occurs partly because of a negative resistance region under those conditions. As shown in this Design Idea, the instability neither arises from the presence of two internal poles, nor from a third pole introduced from an external capacitor in series with the load resistance. A single transistor output stage is added to provide buffering, producing a TTL output level over the entire range. Figure 2 shows the simulation circuit of the TL431.

**Operation of the VCO**

The operation of the oscillator can be understood by considering the circuit in two aspects. The first aspect is the underlying action of the TL431 voltage reference. Consider the equivalent circuit of the oscillator shown in Figure 2. Current I1 (see Figure 3) is a voltage-dependent constant current whose magnitude is approximately equal to (V_{CTRL}-V_{KA})/R (V_{KA} being the “Zener” voltage). Suppose initially that the capacitor is not charged, in which case V_{KA}=0V. The capacitor gradually charges up from a current derived from I1 until it reaches the equilibrium value of the TL431, i.e., V_{KA}=2.49V. Since charging current is still present, the capacitor continues to charge. A transient simulation of the circuit in Figure 2 shows that the capacitor voltage need only exceed the equilibrium value of V_{KA} by a few microvolts for the equilibrium restoring feedback of the device to kick in, as follows:

As the base of Q1 is directly connected to the capacitor, an increase in V_{KA} also increases the emitter voltage of Q1 (which is also the base voltage of Q11), forcing Q11 to conduct more. Transistor Q9 and R8 form the collector load of Q11. A rising collector current in Q11 therefore causes the collector voltage of Q9 to fall. Since Q9 and Q10 are part of a current mirror, the two transistors have the same collector current as Q11, but Q10 has a dynamic collector load made up of Q6, which derives its base current through R5 from the second current mirror made up of the three transistors Q2, Q4, and Q12. This current mirror is configured such that the initial increase in the emitter voltage of Q1 also increases their VBE voltage. This affects Q6 by also increasing its collector current, reinforcing the rising collector current in Q10. Therefore the overall effect is an increase in its collector voltage, which is also the base voltage of the first transistor in the Darlington pair Q7 and Q8, forcing Q8 to conduct heavily, causing its collector-emitter voltage (V_{CE}) which in effect is V_{EA} to fall rapidly. In this particular application the reference terminal (R) to which the capacitor is connected is hardwired to the cathode terminal (K). Therefore, thus far, when the capacitor voltage exceeds the equilibrium, the device tends to rapidly lower its cathode-anode voltage to restore equilibrium.

Figure 3 shows in block schematic form how sustained oscillations start and build up when the internal equilibrium of the TL431 device is disturbed. The capacitor charges from a small, almost constant current that is derived from supply current I1. In Figure 1, this charging current is denoted by I3. When the capacitor passes the equilibrium value of V_{REF} current I2, which is the combined collector currents of Q7 and Q8 in Figure 2, rapidly flows and effectively siphons off charge stored in the
capacitor. The duration of $I_2$ is brief, but is sufficient to drop the capacitor voltage below the equilibrium again. The capacitor then begins to charge from $I_1$ again, and the cycle attains steady oscillation. Since the discharge of the capacitor occurs very briefly, the current during discharge is very much larger than source current $I_1$, according to $I=\Delta Q/\Delta t$, where $\Delta Q$ is the charge acquired by the capacitor during its charging phase.

**Estimation of charging and discharging times**

Since the charging and discharging currents are known, approximate expressions for the charge acquired during charging, and the charge dumped into the output stages of the TL431, can be found. The two expressions are equal during stable oscillation, a process akin to a two step bucket brigade. That is, charge acquired during charging equals charge lost during discharging. In Figure 1, $I_3 = I_1 - I_{\text{BIAS}}$

The magnitude of $I_{\text{BIAS}}$ in the TL431 is about 260 mA over a wide range of $V_{CTRL}$.

From first principles, the following differential equation results:

$$R = \frac{dV}{dl} \approx R_0 e^{-aV_{KA}}$$

The resistance $R_s$ is the series resistance connected to the control voltage. Solving the differential equation from the lower threshold to the upper threshold of $V_C$ during stable oscillation gives the charging time as

$$t_1 = R_s C \ln \left[ \frac{V_{CTRL} - I_{\text{BIAS}} R_s - V_L^H}{V_{CTRL} - I_{\text{BIAS}} R_s - V_L^L} \right]$$

The discharge time is slightly more complex to estimate because the discharge occurs through a dynamic resistance. The effective resistance through which the acquired charge is dumped during discharge can be estimated as follows. Simulations and experiments show that during stable oscillation, $V_{KA}$ does not fall below about 1.60V or exceed about 2.74V. An inspection of the TL431 datasheet, Figure 1, shows how, like a diode, the device exhibits dynamic resistance. This is a diode-like forward bias characteristic that can therefore be approximated by the function

$$I_{\text{BIAS}} = I_0 (e^{aV} - 1) \approx I_0 e^{aV_{KA}}$$

Unlike normal junction diodes, the TL431 current has no significant temperature coefficient since it is designed around a band gap reference. The dynamic resistance can be shown to be

$$R = \frac{dV}{dl} \approx R_0 e^{-aV_{KA}}$$

A linear fit of the datasheet characteristic gave $R_0≈135.9 \, k\Omega$, $a=2.304 \, V/k\Omega$. Hence, in the region of oscillatory behaviour, the resistance changes from 1.7 kΩ to 246Ω. In the context of capacitive discharge this means that as the control voltage increases, the discharge occurs faster since the effective path for discharge has lower resistance. Therefore, one expects that the discharge time will decrease – i.e., frequency will increase as the control voltage increases. This is in fact observed in the practical oscillator. Simulation shows that the discharge involves a large current flowing from the capacitor and therefore the discharge time is typically very short and can be ignored.

The output of the oscillator is directly taken across the capacitor, and external buffering is therefore necessary to prevent loading the capacitor. Other LTSpice models of the TL431 are readily available from a variety of sources – for example, the Texas Instruments website, and the LTspice Wiki. The circuit in Figure 1 was simulated using the different models, and all of them oscillated consistently. In the practical experiments, several equivalents were used from different manufacturers. The TL431A and B, the KA431, and the LM431 were all tried, and though all of them oscillated, the voltage input for oscillation onset and the range of frequency oscillation varied for each. In addition, the reference voltages of the devices were spread from 2.43V to +2.53V.

The output amplitude of the oscillator at the point labelled OSC in Figure 1 is observed to vary as the control input $V_1$ is varied, increasing as $V_1$ increases. Under the currents used in the practical circuits it was observed that the frequency output is about proportional to the control voltage input, but at certain currents, measurements actually showed the same variation up to a certain control voltage (region 1), and then the frequency of oscillation fell as the control voltage is increased (region 2). For the linear region 1, Table 1 gives a sense of the component values and the frequency range versus control input for the different devices tested.

In these experiments the control voltage was limited to about

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**Diagram:**

**Figure 3.** Simple illustration of the current paths in the TL431 relaxation oscillator
In the interest of limiting the cathode currents to 10 mA, although the TL431 datasheet states that the device can sink up to 100 mA. In addition, only the LM431 exhibited region 2, i.e., when the frequency actually decreased with increasing control voltage. This happened between 5.20V and 7.04V control input and a corresponding frequency range of 602 kHz to 433 kHz. The value for C1 was 100 nF. According to the datasheet (Reference 1), the range of capacitance for these instabilities to occur is 10 nF to 100 nF – the same range covered here.

Possible applications include an ultra-low cost laboratory TTL pulse generator and a low-frequency PLL VCO usable in the medium-wave band. The unit was successfully used in a diode-ring mixer circuit to realise a software defined radio (SDR) for the AM band.

REFERENCES:


APPENDIX

LTwiki, The TL431 spice model
Texas Instruments, Spice model of the TL431
Video of the VCO in action
Download the LTSpice files from this link.
The Design Idea in Figure 1 indicates a low-battery condition in an audio test instrument that is powered by four AA cells. As the instrument was otherwise an all-discrete design, this same approach seemed more in keeping with the spirit of the project than the use of a single-sourced integrated circuit.

A garden-variety red LED serves as both the indicator and the voltage reference. A small current through R5 forward biases the LED, but its glow at this low value is barely visible, even in a dark room.

For this application, the LED proved to be a decent reference diode. It has a temperature coefficient that tracks fairly well with that of Q1, and the LED reaches its turn-on knee with less current than a Zener diode needs to maintain its rated voltage. The circuit consumes only 160 µA until it is triggered, at which point the LED runs at 2 mA.

R5 biases the LED to its turn-on threshold, about 1.5V for a red one. This is applied through R6 to the base of Q1. R1 and R2 divide the battery voltage down to about 1.1V at the Q1 emitter. This 0.4V base-emitter differential is below the Q1 turn-on threshold.

As the battery is depleted, voltage across the LED remains constant, but the emitter voltage drops proportionally, and eventually Q1 begins to conduct. This draws base current from Q2, turning it on as well. Additional current to the LED through R4 raises the base voltage of Q1, and this positive feedback snaps the LED on smartly at the alarm threshold. When the LED lights, voltage across it rises to about 1.65V.

Circuit hysteresis is determined by the forward voltage characteristic of the LED, which "stretches" between the small bias current through R5 and the larger illuminating current through R4. But as the battery is not expected to come back to life during instrument operation, hysteresis here is irrelevant.

The RC delay imposed by R6 and C1 slows the circuit latching action. This reduces sensitivity to brief voltage dips from momentary current demands by the load. CR1 was added to discharge C1 when the power switch is turned off, preventing a false alarm should the unit be turned back on suddenly when the battery is partially depleted.

The alarm's trigger point was chosen to guard against biasing and signal headroom issues within the instrument proper. For the values shown, the LED comes on when the battery falls to about 5V. This may be changed by altering the value of R1, or by replacing it with a 100 kΩ potentiometer to afford adjustability. The "BC" series transistors are specified only because they were common to the rest of the instrument; almost any general-purpose devices should perform nicely.
Qi compatible wireless power charging coils

Würth Elektronik eiSos has added three new wireless power charging coils to its range. They have a self-adhesive film on the back to simplify assembly. The coils have flexible ferrite shielding and are 1 mm think. The thin and flexible carrier material is suited for the suppression of interference above 1 MHz. The coils have a high Q-factor and very low DC resistance, for maximum efficiency power transfer of up to 5W. All charging coils have been evaluated and approved with chipsets from Texas Instruments and are Qi compliant. Würth Elektronik eiSos is member of the “Wireless Power Consortium” and of the “Alliance for Wireless Power” (A4WP). The coils are, respectively, 48 x 32 x 0.95mm with inductance of 12 μH, Q-Factor of 33, for 5V operation; 48 x 32 x 0.86mm with inductance of 12 μH, Q-Factor of 21, for operation at 5V; and 38.5 x 30.5 x 0.87mm with inductance of 16.7μH, Q-Factor of 40, for operation at 7V.

Drop-in security for the smart grid comes in a module

ST’s KERKEY secure solution for smart-grid applications provides protection against malicious attack: developed from ST’s smart-card product lines, this ready-to-use solution includes personalisation to use the Java Card operating system, giving flexibility to program application features and implement cryptography functions efficiently. Using the architecture of ST’s secure-processor family, KERKEY embodies a hardware foundation that satisfies CC EAL6+ Penetration Testing for smart-card ICs and FIPS-140 Penetration Testing for Multiple-Chip Cryptographic Modules. Certified to Common Criteria (CC) EAL4+ and AVA-VAN level 5, as well as fulfilling the BSI Protection Profile for smart-grid security modules, KERKEY is the first device of its type to support the Java Card operating system (JC2.2). KERKEY is delivered as a ready-to-use security module that requires only a small amount of final configuration.

Integrated PMIC for automotive instrument clusters

A highly integrated power-management IC from Maxim Integrated combines three high-current DC-DC converters, saving over 50% board space compared to discrete solutions, and reducing board space, noise, and power consumption. Automotive OEMs often limit instrument cluster module consumption to less than 100 μA in standby mode.

Dimmable single-stage 15W LED bulb driver

From distributor Ismosys, Dialog’s iW3609 digital LED driver is designed as the driver for 15W solid-state-lighting (SSL) retrofit bulb applications: it operates with most wall dimmers including leading-edge dimmers (R-type or R-L type) and trailing-edge dimmers (R-C type). The device is a 15W single-stage, AC/DC offline power supply controller for dimmable LED luminaires that require high power factor (PF), low total harmonic distortion, good TRIAC dimmer capability and low BOM cost. The iW3609 detects the dimmer type used, providing dynamic impedance to interface with the dimmer and at the same time control the LED brightness. It uses iWatt’s PrimAccurate primary-side sensing technology to achieve LED current regulation under different AC line and LED load voltages, without using a secondary-side feedback circuit, thereby eliminating an opocoupler. iW3609 key features include: High PF of over 0.92 and Low THD of less than 20%; Proprietary input current shaping option - enables the iW3609 to balance the power loss of the bleeder circuit; Meets IEC61000-3-2 current harmonic requirements and NEMA SSL6 dimming curve standard; Resonant control to achieve high efficiency of over 82% typical.
Level-shifting-logic cuts board space

TI has introduced fully-integrated logic gates with up/down translation: the very wide voltage range logic translation devices reduce board space by more than 50%. The first logic devices to fully integrate logic gate and up/down translation operating from a single power supply, the SN74LV1T family also offers the widest operating voltage range, from 1.8 to 5V: because the SN74LV1T family is 5-V tolerant and supports up to 125°C temperatures, it can also be used in industrial and telecommunications applications as a logic gate, translator or both. This eliminates the need for multiple logic ICs and eases procurement management. The SN74LV1T family is available in nine different logic gates: NAND and AND, NOR, OR and XOR, as well as several different buffer functions.

Silicon carbide FETs boost module efficiency

Power module maker Vincotech has introduced SiC-based products for ultra efficient, high-frequency operation in solar inverter, UPS, and battery management applications. This generation of flow3xPHASE 0 SiC three-phase inverter module with 3x Buck/Boost and split output topology; the other is the flow3xBOOST 0 SiC with three-channel boost circuits. Both modules feature the latest generation of SiC MOSFET switches designed for ultra fast switching frequencies of over 100 kHz. They are able to achieve greater than 99 % peak efficiency at fPWM of 64 kHz. Equipped with integrated DC capacitors, these new flow 0 SiC modules provide ultra low inductance. The flow3xPHASE 0 modules come in low-inductive, 12-mm flow 0 housings with Press-fit pins.

Positioning module uses multiple satellite constellations

Based on MediaTek’s single-chip SoC, Jupiter SL871 is the smallest multi-constellation GNSS in Telit’s range, offering ultra-low standby power for consumer and industrial devices discovering GPS, GLONASS, Beidou, Galileo, QZSS and SBAS constellations. The Jupiter SL871 module uses MediaTek’s low-power MT3333 core, with multi-constellation tracking. It is suited to battery-life sensitive GNSS applications that do not require dead-reckoning, TRAIM and support of communication ports such as USB or CAN bus. The recently introduced companion SL869 V2 module provides these sophisticated features. The SL871 can track GPS + Galileo and GLONASS (or GPS + Galileo and Compass/Beidou depending on the software onboard) constellations, while simultaneously providing positioning data through a standard UART.

“Power SO-8” package cuts PCB area

A series of automotive-qualified transistors offers DPAK-like thermal and electrical performance – on half the footprint. NXP has introduced the first bipolar transistors in the 5 x 6 x 1-mm low profile LFPak56 (SOT669) SMD power plastic package. Six 60V and 100V low saturation transistors offer collector current of up to 3A (IC) and a peak collector current (ICM) of up to 8A. Power dissipation is 3W (Ptot) and low VCESat values yield a thermal and electrical performance comparable to bipolar transistors in much larger power packages such as DPAK, on less than half the footprint. The solid copper clip and collector tab design of the NXP LFPak package is the basis for achieving this high power density, as it reduces the package’s electrical and thermal resistance significantly. The LFPak56 bipolar transistors are AEC-Q101 qualified and suitable for a wide range of automotive applications in an ambient temperature of up to 175°C through a standard UART.

Module mixes WLAN 802.11ac, Bluetooth 4.0 and NFC

Distributor MSC Technologies has an automotive-grade wireless module from Lesswire; the WiBear11ac, with dimensions of 15 x 20 x 2.5 mm, combines WLAN 802.11a/b/g/n/ac, Bluetooth 4.0 and 2.1 as well as NFC on a single module. The module is designed for both simultaneous and independent operation of the different technologies. The module can be connected to a host controller by means of SDIO interface. In addition to a Bluetooth interface, a UART interface is available for Bluetooth operation. A two-wire serial interface (TWSI) is included on the module for near field communication (NFC). Audio applications are supported by integrated PCM and I2S functions. Through the 1x1 antenna configuration, PHY data transfer rates up to 433 Mbps and transfer rates up to 3 Mbps via Bluetooth are feasible. You can add 64-bit or 128-bit AES hardware encryption and integrated security mechanisms such as 64/128-bit WEP, WPA, WPA2 and WAPI.

www.edn-europe.com
Bluetooth Smart dev kit for Arduino-based projects

Nordic Semiconductor has a development kit that adds Bluetooth Smart capabilities to the Arduino platform. The Bluetooth Smart SDK ports the nRF8001 SDK to an Arduino-compatible set of libraries. The SDK will be provided as an open-source repository on GitHub for use, modification, and expansion by developers. The SDK is compatible with a range of Arduino, ChipKIT shields that employ the nRF8001 Bluetooth Smart connectivity device. The Bluetooth Smart SDK is a port of the existing SDK available for the nRF8001 Bluetooth Smart connectivity device. The SDK contains many different examples including: Human Interface Device (HID); UART over Bluetooth low energy; Heart Rate Monitor (HRM); Temperature; and Proximity. The software interface for the Bluetooth Smart SDK for Arduino has also been implemented on a variety of microcontrollers and microcontroller platforms such as ChipKIT, Maple, Teensy, mbed, and others.

Improved model-based code quality

Dspace has announced that it is co-operating with AbsInt Angewandte Informatik GmbH, which becomes a member of its TargetLink Partner Program. The two companies are working together to couple AbsInt analysis tools – aiT, StackAnalyzer and Astree – with the dSPACE TargetLink production code generator. Timing errors, stack overflows and run-time errors due to erroneous model specifications can now be analysed directly from within the TargetLink model and detected reliably in early development phases. Analyses can be configured to be largely automatic to provide more precise results. The tool coupling combines model-based software development with the verification of nonfunctional requirements at the implementation level. It will provide seamlessly integrated development from model design, to production code generation, to certification, thereby, reducing development time while also enhancing software quality.

EMI absorption material cuts radiated noise

Molex’ HOZOX Electromagnetic Interference (EMI) Absorption Tape and Sheets provide a means by which manufacturers of high-frequency equipment in multiple industries, including medical, consumer electronics, data/telecommunications and microwave/radio frequency can control radiated emissions. HOZOX absorption technology employs a unique dual-layer design to maximise the EMI noise mitigation performance. The magnetic layer’s powder composite absorbs lower frequency electromagnetic energy, while the conductive layer’s powder and high loss dielectric resin absorb high frequency electromagnetic energy. The products feature a very thin form factor and come in two different tape formats as well as an A4 sheet format, all of which can be easily die-cut to specific configurations.

ST shows digital lighting control chip in a high-efficiency street lighting design

STMicroelectronics offers a design around its STLUX385A digital controller for lighting and power-conversion applications, which it says enables “Jump-start[ing] municipal savings by accelerating street-light conversions... new possibilities for high-power/street-lighting LED applications pave the way to smart cities.” The design helps optimise LED lamp efficiency at any dimming level and minimise power in idle conditions. The complete and configurable solution allows designers to develop and efficiently control a dimmable, high-brightness LED string (up to 100W) for street-lighting applications. Based on ST’s STLUX385A digital power controller, the street-lighting plug-and-play design highlights the device’s ability to optimise LED efficiency at any dimming level and minimise power in idle conditions. The reference design includes full schematics, bill of materials and firmware, enabling you to rapidly develop digital power controllers for 100W LED lamps.

Run logic direct from 48V distribution

A pair of high voltage linear regulators is designed for use in 48V DC power systems in telecom, networking and Power-over-Ethernet equipment. Integrating several components into TO252-4 and PowerDIS060-8 packages, the ZXTR1005K4 and ZXTR1005PD8 help minimise circuit footprint while providing a fixed 5V (±2%) output and a high drive capability of 50 mA. For high voltage regulation tasks, where industry standard linear regulators can’t be used, the ZXTR1005 provides a cost effective alternative that offers a significant improvement in supply reliability. The regulated 5V output enables microcontrollers to be powered from 48V telecom rails, while the devices’ 100V-tolerant inputs cope with any transient conditions. The ZXTR1005K4 (TO252-4) and ZXTR1005PD8 (PowerDIS060-8) are priced at $0.30 (10,000).
More accurate battery “fuel gauging”

Infineon’s ORiga 3 enables accurate fuel gauging in mobile devices; its PrediGauge technology chip meets MiPi BiF standard. In order to accurately determine its charging state, the battery needs to relax in a no-load condition between one and two hours. Only then can the Open Circuit Voltage (OCV) be used to re-calibrate the fuel gauge and correct errors. However, functions such as internet browsing, navigation, and video streaming along with self-updating apps such as Facebook and Twitter lead to almost constant power consumption while charging cycles become shorter and more frequent. ORiga 3’s PrediGauge technology improves consumer satisfaction by accurately determining remaining battery capacity under these most adverse conditions. Within a few minutes of battery relaxation it predicts the future OCV and therefore the charging state within an average accuracy range of 1%.

CMOS multi-standard/multi-band MIMO transceiver

Lime Microsystems has announced its second-generation field programmable RF (FPRF) device, the LMS7002M, built in 65nm CMOS technology to reduce the cost of FPRF transceiver technology and significantly reduce power consumption. The chip integrates 2 x 2 MIMO functionality and significantly extends the spectrum coverage compared to its predecessor. The LMS7002M supports all cellular standards and frequencies, including 2G, 3G and 4G / LTE and their TDD / FDD variants amongst numerous other standards such as WiFi; use it, Lime says, in a broad range of consumer and professional applications. The company believes that the flexibility, low power consumption, functionality and price of the LMS7002M FPRF, makes it an “exceptionally disruptive entry” to the transceiver chipset market, offering an advanced transceiver function for a fraction of the cost of existing solutions. You can also “pin-out” connections to use individual functions of the chip in isolation.

Multiprotocol transceiver for all traditional serial standards

With internally switched termination, and occupying a 5 x 5 mm package, Exar’s SP335 multiprotocol transceiver supports RS-232, RS-485, and RS-422 serial standards. At 5 x 5 mm, the SP335 is less than half the size of a comparable discrete design, doubling the number of serial interface channels that can be assembled in the same board space and allowing you to combine multiple serial protocols over the same connector. Programmable end-of-line termination and multiple configuration modes allow all three protocols to be used interchangeably over a single cable or connector with no additional switching components. The SP335’s bus pins are protected against ESD events exceeding ±15 kV IEC 61000-4-2 Air Gap Discharge, and ±8 kV IEC 61000-4-2 Contact Discharge, and can tolerate direct shorts to DC or AC voltages as high as ±18V.

Motion-tracking IC implements dead-reckoning

Swiss company u-blox has introduced an IC for advanced in-dash navigation, emergency call such as eCall and ERA-GLONASS, usage-based insurance (UBI), road-pricing, and stolen vehicle recovery systems. The UBX-M8030-Kx-DR chip integrates 3D ADR technology (3D Automotive Dead Reckoning), which enables it to calculate a vehicle’s position, speed, as well as elevation in areas of poor or no satellite visibility, a common scenario in high-density urban environments, stacked highways, or parking garages. The technology aids traditional GNSS navigation systems such as GPS, GLONASS and BeiDou by blending them with individual wheel speed, gyroscope and accelerometer information to maintain accurate 3D positioning even when satellite signals are completely lost. The UBX-M8030-Kx-DR chip is self-calibrating to compensate for sensor aging and temperature effects.
I am an electrical engineer for the manufacturing department of a defense company. We build custom test stations for our products. Some time ago I had to build a test station that was essentially a copy of another test station we built a number of years earlier using VXI test technology. One instrument on both stations was a microprocessor-based combination UART transceiver and digital I/O circuit card plugged into the station’s VXI rack. There were four of these devices. The UART/DIO card was a 68000 microprocessor, and the original engineer wrote the assembly language code to make them function.

In the test station the UART section was to receive a short 9600 baud serial data message and then respond with a short, but different, 2 Mbaud serial data message back. However, the 2 Mbaud signal was too odd of a baud rate and too fast for the UART transmitter to handle. So the clever engineer decided to use the digital I/O section to “bit push” the 2 Mbaud message from one bit of the digital output port, after he changed the clock crystal to generate the 2 Mbaud rate. Essentially, his program just wiggled the output bit port high and low with the usual start bit, eight data bits, a stop bit, and parity bit. It worked beautifully.

However, on the copy station I built, the new UART/DIO circuit cards I bought for it worked intermittently. Out of the four, only one worked all the time, so we bought three more. They were intermittent as well. We called the manufacturer of the cards and they told us that no changes were made to the units between the ones we just bought and the ones we bought some years ago. I told them how we were using it, but they couldn’t find anything wrong.

Eventually this problem stretched to almost a year without a solution. I had to learn the assembly language of the device, but since I didn’t write it I didn’t have a deep understanding of it. I told myself, after being so frustrated over it, that I was going to have to be the one who solved the problem. No one else was going to do it. I finally took one more look at the code, which thankfully was well commented by the original engineer, and noticed something. His comment next to a particular command was “Enable UART transmitter and receiver.”

It finally struck me. Why was the transmitter UART being enabled when we weren’t using it? We were using the receive UART, but the transmit UART was not able to do 2 Mbaud, so we used the digital output bit instead. I changed the command to disable the transmit UART, recompiled the code, loaded it in the card, and tried it. Lo and behold the intermittent problem went away. Whew! After a whole year it was finally fixed.

For some reason there was a slight manufacturing difference in the units we just bought and it just didn’t like the transmitter section being enabled during receive mode. It shouldn’t have mattered: but it did. It wasn’t at all obvious. Thankfully the code was well commented, and gave me the clue to fix it.

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