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WW Share No.1 in photocouplers

We will continue boosting production to bring these devices to the world.


Toshiba’s photocouplers

Thanks to the low power consumption, small and thin package size, and variety of line-ups, Toshiba’s photocouplers have earned the world’s highest sales revenues. From 2013, we began operating a new factory in Thailand to reinforce the stable supply of these high quality devices at a lower cost.

Toshiba Semiconductor & Storage Products

http://www.semicon.toshiba.co.jp/eng/product/opto/ coupler/index.html
A utonomous, or self-driving, cars; are they still largely science fiction, or are they closer to market reality than many of us appreciate? Everyone has by now seen the output of Google's very able PR machine, in the form of footage of its autonomous car navigating the freeways and urban streets of California. Impressive though it is, it is a vastly complex machine and is unlikely to represent the form in which the average consumer will be offered self-driving capabilities. Make that; is already being offered those features. Autonomy will not arrive in one spectacular product launch, but as an increasing range of functions that the human driver will have the option of selecting. Automatic parking, or park-assist is already in place in many current models; lane departure warning is already morphing into lane departure correction (where the vehicle intervenes as well as alerting) – the revolution is under way. Even if we’re not sure what the revolution should look like.

This is not so much about the technologies: we know, for the most part, how it will be done, and where the development is needed. The building blocks start with radar, lidar, imaging, image processing – everything that allows the car to place itself in its environment. Add the means to communicate with that environment – vehicle-to-vehicle and vehicle-to-infrastructure. Add the software – Oh! The software! Recall that one of the biggest stories of 2013 was the outcome of the US lawsuit concerning the Toyota ECU software: how will we ensure that an entire autonomous vehicle’s suite of software is up to safety-critical-systems standards? How to protect it from hacking? Or to maintain privacy when constant communications to “the network” will be implicit?

As I said, it’s not really about the tech; it’s about ourselves – how do we feel about ceding control of our road journey to the systems, how do we handle the legal framework? When it goes wrong, where will the fault lie?

Marketing self-driving cars will be a challenge for the image-makers, every bit as much as it is for the technologists. The car is sold as life-style accessory, as an exciting extension of our personalities: the manufacturers sell us the glossy image of freedom and a life on open, deserted roads. In reality what we buy is the means of commuting in rush-hour traffic or – even more prosaically – an extension of the shopping trolley between the supermarket car-park and our own driveway. Even more of a challenge for the marketing department is that ever-more R&D gets poured into producing what will become, or potentially might become, little more than a personalised taxi. If you (as consumer) take that mental leap of depersonalising the act of driving, will you still be susceptible to being sold the up-market image, and be prepared to buy the higher-range model configurations where the industry currently makes its margins?

We can see that the car-makers are already alert to this issue. It was widely reported that at this year’s Consumer Electronics Show, BMW released details of a prototype that will maintain automated control even in the circumstances of a high-speed “drift” through a corner. Calling it ActiveAssist, BMW says that the feature can bring a vehicle “back into line in demanding driving situations without any input from the driver”. The message is clear; have no fear, you can buy into all the self-driving technology and still have the “driving experience”. Can the marketers succeed with that? - only time will tell.

You can take this topic in any number of directions and here, I’m trying avoid the pure technology aspects. For example; there is a fundamental, almost philosophical, issue that – it seems to me – has scarcely been addressed at all. Step forward, in your imagination – and leave aside for now how far away in time you happen to think that will be – and carefully set to one side that very word “autonomous”. Ask, rather, is that future a vehicle-centric model, or is it infrastructure-centric? Does each car effectively fend for itself, each monitoring and responding to the actions of every other car around it, as well as to its environment? Or must we develop an over-arching road-management infrastructure in which I hand over control to the car, only to have it, in turn, surrender to a higher level of authority?

Already, I detect a shift in thinking and presentation about how the industry would have us view the automated systems on offer now, or coming soon. Early discussions would always assume the context of a car “on autopilot” in which the human driver would always be able to take back control should things go wrong. Recently, the emphasis has shifted – if you are cruising at speed on the motorway/freeway/autobahn and something fails, it is the system that will intervene to guide the car to a halt in the safety lane/shoulder. That may seem a small change, but is actually an inversion in thinking about who is ultimately in control.

Any discussion of the topic can quickly become surprisingly emotionally charged. Even among groups of industry insiders, I have heard opinions that polarise into, “I wouldn’t trust myself to one of those,” right through the spectrum to, “Bring it on, it cannot come fast enough for me.” Personally, I lean to the latter viewpoint; I have spent many years in which family members were located at opposite ends of the UK, and have driven many thousands of kilometres on the country’s motorways. If, over those years, I could have engaged “freeway auto mode” as I left the south of England, and taken back control 400 km later when I left the motorway network in Scotland, I would have been only too happy. Which goes back to where I started; you don’t need the entire autonomous function set to offer a viable product. A combination of lane-following, collision-avoidance, speed-control and radar separation would have sufficed for my situation. And, barring legal constraints, I could have that today. While we marvel at Google’s video, the industry is going to deliver self-drive, piece-by-piece, around us. Even those of us with heads-down, working at refining the sub-systems, may be taken by surprise.
1.2 kW from a 63 x 23 mm converter – and it is bi-directional

Vicor’s first ChiP power modules are 380 VDC input bus converter modules that enable high voltage DC distribution with 98% efficient conversion to 48V at 1880 W/in³ power density. Claiming 4x the density of competing solutions, this will enable efficient, high voltage DC distribution infrastructure in datacentre, telecom, and industrial applications, Vicor says.

In mid-2013, Vicor described the construction of the next step in its miniaturisation of power conversion modules, without announcing product details; now, the company has issued the first such specification, for the ChiP (converter housed in package) bus converter module (BCM). BCMs are fixed-ratio isolated DC/DC converters: in effect, they are “DC transformers”. The ChiP BCM takes the analogy of transformer operation one step further in that the symmetry of its internal circuitry means that it can operate bi-directionally – power flow can be in either direction.

The 63 x 23 x 7.3-mm device is a 1/8 ratio converter that will deliver 1.2 kW (1.5 kW for 10 msec) with only airflow cooling; the rating is thermally, not electrically limited and appropriate cooling will enable higher ratings, Vicor says. With a nominal input voltage of 380V and a K-factor of 1/8, the converters supply an isolated 48V distribution bus with a peak efficiency of 98%. With its input range of 260 to 410 V, the new BCM supports outputs ranging from 32.5 V to 51.25 V. BCMs are based on Vicor’s ZCS/ZVS (zero-voltage/zero-current switching) Sine Amplitude Converter topology and operate at a 1.25 MHz switching frequency, providing fast response time and low noise operation.

ChiP BCMs may be paralleled to provide multi-kW arrays and are capable of bi-directional operation to support battery backup and renewable energy applications. Standard BCM features include under-over-voltage lockout, over-current, short circuit and over-temperature protection. ChiP BCMs incorporate digital telemetry and control features that can be configured to meet customer requirements.

Module construction uses highly-automated assembly, on large panels. Heat-dissipating components are mounted symmetrically on either side of the substrate, and magnetic components mount through the substrate, with their top and bottom surfaces exposed at the surface of the over-mould. The complete panel of assembled modules is over-moulded, then sawn as if it were a giant silicon wafer. The dimensions of the sawn converter modules are incorporated in the part numbers, in mm. Exposed connections at either end of the module (picture) receive terminations to allow normal through-hole interconnect (pins) to be added; surface mounting assembly options will be offered at a later stage. Vicor says that directly connecting the modules to the exposed-edge connections, and mounting the converters in a board cutout, is a possibility, but not one that is yet offered.

You can operate the modules with no heatsinking, or with one- or two-sided heatsinks. Advanced designs for use of the devices have already been developed that apply a pressure contact to each side of the converter (illustrated), with liquid-cooling to conduct away heat. The modules use, “advanced magnetic structures integrated within high density interconnect (HDI) substrates with power semiconductors and control ASICs,” Vicor says; however, the semiconductor switches are still silicon MOSFETs – the advantages come from circuit design and packaging, and not from use of exotic technologies or materials.

Vicor’s 6123 VI ChiP BCM costs $120.00 in OEM quantities.

Vicor
www.vicorpower.com
Your question: EMI debugging with oscilloscopes?

Our answer: Yes, you can! With digital oscilloscopes from the EMC expert. The R&S®RTO digital oscilloscope is a valuable tool for analyzing EMI problems. Using near-field probes, electronic design engineers can quickly understand unwanted emissions and identify their causes.

Your advantages at a glance:
- High-speed, easy-to-use FFT
- Wide dynamic range and high sensitivity of 1 mV/div
- Color-coded display of the frequency of occurrence of spectral components to reveal intermittent signals
- Correlated time-frequency analysis with gated FFT
- Frequency mask for capturing sporadic events

See for yourself: www.scope-of-the-art.com/ad/emi

Please visit us at the Embedded World in Nuremberg, Hall 4, booth 4-611
16-channel, 14-bit ADC fits medical imaging applications

A D9249 is a 16-channel, 14-bit, 65 Msps analogue-to-digital converter (ADC) with an on-chip sample-and-hold circuit that is designed for low cost, low power, small size, and ease of use. The device operates at a conversion rate of up to 65 Msamples/sec and is optimised for dynamic performance and low power in applications where a small package size is critical. Use it, ADI suggests, in medical imaging, communications receivers and multichannel data acquisition.

The ADC requires a single 1.8 V power supply and an LVPECL-/CMOS-/LVDs-compatible sample rate clock for full performance operation. For many applications, no external reference or driver components is required.

Features include;
- SNR: 75 dBFS (to Nyquist); SFDR: 90 dBc (to Nyquist)
- DNL: ±0.6 LSb (typical); INL: ±0.9 LSb (typical)
- Crosstalk, worst adjacent channel, 10 MHz, −1 dBFS: −90 dB typical
- Small footprint; sixteen ADCs are contained in a 10 mm × 10 mm package.
- Power of 35 mW/channel at 20 Msamples/sec with scalable power options (for example, 58 mW per channel at 65 Msamples/sec)
- Ease of use; data clock outputs (DCO±1, DCO±2) operate at frequencies of up to 455 MHz and support double data rate (DDR) operation.

Analog Devices

Precision Power Scope combines power-analysers and 'scope measurements

Yokogawa has tightly-integrated power-analyser and oscilloscope technologies to create what the company believes is a new class of instrument, that will add the time-based approach of the scope to the detailed power analysis of a dedicated analyser.

The PX8000 takes the form of a mainframe that hosts up to eight measurement modules. The mainframe is essentially a digital host platform that presents oscilloscope-style waveform displays, of either measured or calculated parameters, and/or numerical values (voltage and current, or power, harmonics, or a broad range of power-related figures); or graphical trend information extracted from the basic measurements.

Each measurement module (there are three at launch; voltage, current and sensor/auxiliary inputs) is a measurement sub-system with sampling at 100 Msamples/sec, and 12-bit A/D conversion, that passes timed measurements across an optical isolation barrier to the host unit. You use V and I modules in pairs, to provide data sets for power computations. The input modules cover voltages up to 1000 V RMS and currents up to 5 A RMS (higher values are possible with external current sensors), with basic accuracy down to ±0.1%. The analogue bandwidth, viewed as a scope-style system, is 20 MHz for voltage, 10 MHz for current. The instrument can compute harmonics up to the 500th, based on a fundamental of up to 6.4 kHz, as well as a broad range of other parameters such as power factor, efficiency and distortion.

You can use all of this functionality together with the waveform display; if you place start and top cursors on the waveform (of a stored, captured waveform) the instrument will calculate the suite of power measurements over that exact interval. Combined with an advanced triggering facility, with logical combinations of trigger conditions, this enables detailed power analysis of transient conditions that would be very difficult with a combination of conventional oscilloscope and power analyser, Yokogawa asserts, referring to, “…high-accuracy time-based power measurement: a need that conventional power analysers and oscilloscopes were never designed to meet.” Optical isolation allows safe operation of the instrument when the measured voltages may be far above ground.

A variety of functions including arithmetical calculations, time shifting and Fast Fourier Transforms enable users to display waveforms with offsets and skew corrections. An automatic de-skewing function eliminates offsets between current and voltage signals that may be caused by sensor or
Versatility...

The Tektronix 500 series was introduced in the 1940s. Since then, breakthroughs have been a part of our legacy. The Tektronix Type 547 Oscilloscope was a product of its kind: it can display frequency and time domain data together, which greatly simplifies debug on devices with integrated RF.

For quality products and traditional values, trust Tektronix.

Breakthrough

An industry breakthrough in the field of electronics is the Mixed Domain Oscilloscope (MDO). The MDO is the world’s ONLY oscilloscope that can display frequency and time domain data together, which greatly simplifies debug on devices with integrated RF.

Win a MDO4000B!

Do you have the oldest, working Tek scope? Go to uk.tek.com/oldestscope and register your instrument’s details. You could win the brand new MDO4000B!
Microchip’s MCP39F501 is a power-monitoring IC that embeds high-accuracy signal acquisition and power calculations, with digital data output. The chip carries out real-time measurement of AC power with 0.1% error across a 4000:1 dynamic range, with integrated power calculations and programmable event notifications; use it in consumer, commercial and industrial products.

The chip has the expected architecture of a voltage input channel and a current channel that senses voltage across a series shunt resistor in the load current path. Each has a 24-bit delta-sigma ADC, that feed a 16-bit calculation engine, EEPROM and a flexible two-wire interface. An integrated low-drift voltage reference in addition to 94.5 dB of SINAD performance on each measurement channel yields the 0.1% error and 4000:1 dynamic range figure. Inputs are scaled to be in the ±1V range, and the typical-application data sheet shows shunt resistors in the 0.5 – 4 mOhm range.

As it is directly connected to the load lines, isolation is needed, that you can provide by opto-couplers in the digital path to (and from) a microcontroller. The chip has an operating temperature range of -40°C to +125°C that allows it to be used in more extreme environments: it comes in a 28-lead QFN 5 x 5 mm package. It is supported by the MCP39F501 Demonstration Board (ARD00455) priced at $89.99.

1-chip, 0.1%-accurate AC power monitoring uses low-loss mΩ shunts

Providing up to 2 GHz of information bandwidth, TI says its 4-channel, 2.5-GSample/sec DAC38J84 is 66% faster than competition and supports the JEDEC JESD204B serial interface standard for data converters up to 12.5 Gbps. The pin-compatible 2-channel, 16-bit DAC38J82 also runs at 2.5 GSPS, 25% faster than existing 16-bit dual DACs.

TI designed the DAC38J84 and DAC38J82 to provide the bandwidth, performance, small footprint and low power consumption needed for multi-mode 2G/3G/4G cellular base stations to migrate to more advanced technologies, such as LTE-Advanced and carrier aggregation on multiple antennas. The DACs support up to 2 GHz of information bandwidth for wideband power amplifier digital pre-distortion, millimeter wave backhaul infrastructure, signal jamming, radar and test equipment.

An interoperability report is available demonstrating the DAC38J84 with Altera’s Stratix V and Arria V FPGAs. The report provides the guidance designers need to quickly implement a working link between the FPGA and high-speed DAC.

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Chip makers put Bluetooth Smart chips and devkits into the market

Designers embarking on a project with Bluetooth Smart connectivity have gained new development options from two suppliers.

Toshiba has a starter kit for users of its TC35661SBG-501 (“Chiron-501”) Dual Mode Bluetooth IC (BT 4.0). The starter kit (BMSKTOPASM369BT) is based around a Panasonic PAN1026 module featuring an embedded “Chiron-501” IC with a dual mode Bluetooth protocol stack and profiles and includes a Toshiba TMPM369 ARM Cortex-M3 based MCU with 512 kB flash memory.

The embedded dual mode software has a high level Serial Port Profile (SPP) and Bluetooth Low Energy (LE) GATT API for device set up, connection and data transfer. A high level driver layer allows access to the function set of the Bluetooth IC. Application examples are provided on the internet that can be compiled to run on the TMPM369 MCU with FreeRTOS integration (OS itself is available from Real Time Engineers Ltd). The application software includes a set of BLE standard reference profiles and a design guide on how to develop a proprietary BLE profiles.

A J-Link JTAG debugger interface incorporated in the starter kit board is compatible with commonly available third party toolchains such as those from Atollic, IAR and Keil. The embedded MCU also supports standard interfaces on the board for Ethernet, CAN, USB (host and device), serial and UART connection.

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Toshiba Electronics Europe
www.toshiba-components.com

Claiming it as the world's smallest and lowest power device in its class, Dialog has placed its smartBond Bluetooth v4.0 smart SoC, targeting wearable, sport & fitness, medical and computing applications, into volume production.

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Claiming it as the world's smallest and lowest power device in its class, Dialog has placed its smartBond Bluetooth v4.0 smart SoC, targeting wearable, sport & fitness, medical and computing applications, into volume production.

The DA14580 SmartBond SoC, with a variety of analogue and digital interfaces and including an embedded ARM Cortex M0 processor, has the lowest power available with less than 15 mW active, 600 nA standby current, and with the smallest package sized at 2.5 x 2.5 x 0.5 mm, is half the size of competing solutions.

It has now passed the Bluetooth Qualification process, meeting the requirements of the Bluetooth v4.0 specification, which ensures interoperability. The DA14580 is now officially listed on the Bluetooth SIG site as a certified Bluetooth controller subsystem and host. The Qualified Design ID (QDID) is used by end customers as part of their product listing when putting a product on the market. The qualification allows Dialog customers to use Dialog's QDID status to simplify their own qualification process.

SmartBond is designed to enable consumers to use innovative new apps on their smartphones and tablets that can easily connect with watches, fitness-bands and monitors, medical, sporting remote control, computer peripherals and other applications. Dialog has worked with a number of module manufacturers including Panasonic Industrial Devices Europe to develop tiny modules allowing product designers with little RF expertise to rapidly create unique Bluetooth Smart applications. Panasonic selected the DA14580 for its next-generation Bluetooth Smart modules, which are expected to launch in the first quarter of 2014.

A complete development kit which enables quick and easy product development is available at the Dialog website. The DA14580 is also delivered with SmartSnippets, a comprehensive tool suite which integrates a fully qualified Bluetooth Smart single mode stack supporting both master and slave roles.

Dialog
http://support.dialog-semiconductor.com
Controller handles currents up to 300A by adding regulation phases

TC3874 is a dual phase synchronous step-down slave controller that generates currents up to 300A, when paired with a companion master controller, by extending the phase count in multiphase applications. Compatible master controllers have true current-mode control and enable the use of low (0.2 milliOhms) DC resistance (DCR) power inductors — without any sense resistor — to maximise converter efficiency and increase power density.

The LTC3874 works with Linear Technology’s low-DCR peak current mode controllers and provides all functions needed for multiphase slave designs, including accurate phase-to-phase current sharing, even for dynamic loads. It operates over an input voltage range of 4.5V to 38V and produces a fixed output voltage up to 5.5V. Up to 12 phases can be paralleled and clocked out-of-phase to minimise filtering. Applications include power distribution, redundant (n+1) supplies, industrial systems, DSP and ASIC power.

The LTC3874 has a fixed operating frequency from 250 kHz to 1 MHz or it can be synchronised to an external clock. The 1.1-Ohm onboard gate drivers minimise MOSFET switching losses. Precise programmable current sense threshold limits from 16 mV to 72 mV minimise power loss and accurately set the over-current trip point. Additional features include selectable continuous or discontinuous light load operation, programmable phase shift control and overvoltage protection.

The LTC3874, in a 28-lead 4 x 5mm QFN package, costs $2.47 (1,000).

Linear Technology
www.linear.com/product/LTC3874
High-performance processors enable continuous improvement in many sectors, including the medical device market. The driving force behind microprocessor evolution has, for decades, primarily been the needs of the IT sector and personal computing, the roadmap provided by leading manufacturers has guaranteed allegiance to a common architecture; support that has been mutually beneficial to all.

As the needs of traditional applications broadened, processor manufacturers responded, by extending and enhancing the core architecture while retaining code compatibility, allowing for easy migration as more powerful solutions became available. While the capabilities and functionalities evolved, however, one parameter above all others had to be preserved; increased performance. As a result of constant improvement in their performance, over the last decade or so these same processors have slowly but inexorably migrated to other applications, delivering a level of performance that now enables many established and emerging applications.

More recently the need to deliver that performance within tighter power budgets has become apparent, the cost of greater performance has traditionally been increased power, but as integrated circuits become more power-hungry their ability to dissipate the subsequent heat diminished. The performance they could provide was becoming physically limited by the power needed to deliver it, a trend that was unsustainable. In a bid to overcome this impending roadblock processor manufacturers had to radically re-engineer their fundamental manufacturing processes, a difficult challenge but one that has ultimately resulted in even greater architectural innovations; each one widening the sphere of potential applications.

The medical sector is one of the many applications that has benefited from processor innovations and greater focus on the particular requirements of the embedded market. Subsequently many of the features we have become accustomed to in one market are now being made available in others, providing the same productivity gains and improved user experiences.

Medical devices, for example, are predominantly designed to be uni-functional; perform one task very well. Their ability to perform that task — the efficacy of the device — can be measured by the quality of the results and in health care there is no such thing as ‘good enough’; when it comes to diagnosis or health care administration there’s always room for improvement.

In medical devices, this translates to greater capability in uni-function devices, thereby raising the overall efficacy of the equipment. What may have once required several processors attempting to work together can now be accomplished on a single platform running more sophisticated software with greater efficiency.

**HSA & OpenCL**

The trend to integrate more cores and capability into general purpose microprocessors has significant benefits in the medical sector. Graphics processing units are fundamentally very powerful co-processors that run in parallel to each other and the main processor. As a result they can, in principle, be applied to any massively parallel data processing tasks.

Using graphical processing units for ‘general purpose’ tasks is an emerging trend and has become known simply as GPGPU. Medical imaging equipment generates vast amounts of data, all of which needs to be processed, and so GPGPU is particularly applicable in this application.

GPGPU is enabled by a number of open source software projects such as OpenGL and OpenCL, that allow algorithms to be ported to practically any processing architecture; important because graphics processors are typically designed for maximum performance at the cost of architectural continuity. The OpenCL project uses a level of abstraction that allows algorithms to be ported to any architecture that supports the language and it has rapidly become the ‘default’ approach for GPGPU.

Using GPGPU in medical applications makes sense, because it allows data that is easily parallelised to be processed in a more efficient flow. Established processor architectures, even multicore processors, are typically executing software written in C, which doesn’t inherently support parallelism; while many tasks can be executed simultaneously, even the same task, GPGPU is better suited to raw ‘data crunching’. This increased throughput can have a direct impact on the efficacy of medical imaging equipment or any device that relies on processing raw data as it’s acquired, in real time.

The continuation of this article describes some specific devices that embody these trends, and looks at the impact of the Heterogeneous System Architectures (HSA) Foundation.
I’ve had a couple of pieces of networking gear fail in recent weeks; I’ve decided to “turn lemons into lemon-ade” and dissect them for your (and my) enjoyment and education. First on the list is TRENDnet’s TEG-S8, an eight-port GbE switch which was in production in the latter part of the last decade (in May 2008, for example, it was promotion-priced at $15) but has now been discontinued (here’s the associated product support page). The TEG-S8 was notable not only for its aggressive pricing but also for its performance-boosting jumbo frame support, and it served me well (albeit only periodically ... I’d phase it in and out of service as my residence locations and network topology needs evolved) for many years.

Recently, however, a few remotely accessible LAN clients mysteriously went offline while I was away on a trip. Upon my return, I noticed that all of the TEG-S8’s front panel “link” and “activity” LEDs were extinguished (echoing an experience I’d had nine months earlier); only the “power” LED was still illuminated. I power-cycled the switch and it came back to life ... for a few minutes, at least, until the unwanted switch slumber re-turned. A few more power cycles resulted in the same undesirable end result, at which point I decided it was time to transition to a switch successor.

Removing four underside-accessible Phillips head screws is all it takes to pry apart the TEG-S8’s plastic case. At the top of the following photo, you can see the eight metal-shielded Ethernet ports, with the TEG-S8 power plug to their left:

Below them, you’ll notice four SOIC-packaged ICs; I thought “DRAM” when I first saw them. A Google search quickly revealed, however, that they’re 1000-Base-T LAN transformers (the G4802CG, to be precise, from Dongguan Mentech Optical & Magnetic), one per two ports. Ironically, however, memory represents the TEG-S8’s fundamental shortcoming versus successor-generation products from both TRENDnet and other suppliers. The TEG-S8’s diminutive 8 kByte buffer could be insufficient when, for example, shuttling packets between GbE and 100 Mbps clients. Take a look at TRENDnet’s now-shipping 8-port GbE “Home Products,” in contrast, and you’ll encounter buffer sizes ranging from 128 kBytes to 256 kBytes.

The other object in the system board’s top-side photo that will likely catch your eye is the heatsink in the lower centre, directly above the multi-LED array. SmallNetBuilder’s review says that underneath it is Broadcom’s BCM5398 eight-port switch single-chip controller with integrated PHYs (quick aside: Broadcom and foundry partner UMC announced what they claimed was the “world’s first 8-Port Gigabit Ethernet switch-on-a-chip,” the BCM5680, back in May 2000). Thank goodness for Small-
NetBuilder’s IC insights; I wasn’t able to pry the heat sink away from the device underneath it in a way that I felt confident would preserve the package markings, and although TRENDnet claims that the TEG-S8 “has been tested and found to comply with FCC and CE Rules,” I couldn’t find a FCC ID either on the device itself or its packaging or documentation, which might lead to a bill-of-materials report:

The TEG-S8’s system board bottom side is far less exciting, befitting a cost sensitive, therefore highly integrated, consumer electronics device:

So what happened to the TEG-S8? One possibility that comes to mind is that the “wall wart” power supply is failing, and its diminished current and/or voltage output is inhibiting full operation. I suspect however, that extended exposure to high ambient heat might be behind the TEG-S8’s demise. I’d located the switch in the middle of a three-device stack, in-between my Cisco Linksys E4200 v2 router (below it) and DPC3008 cable modem (above it). Although I’d been careful to not obscure any of the three devices’ airflow vents, their close vertical proximity may have still led to the TEG-S8’s internals getting “cooked.” While most of the time when we speak of “power consumption” we’re thinking of electrical bill impacts, it’s also important to consider the potentially formidable thermal effects of power draw excess.
FIVE KEY CHALLENGES TO IMPROVING LTE NETWORK BACKHAUL SPEED - AND HOW TO SOLVE THEM

The move to LTE brings great improvements in connection speeds (30 Mbps typical) but it also brings a costly problem with it; the need to greatly uprate mobile network backhaul speeds. Today’s average backhaul capacity is 35 Mbps per cell and this needs to increase to approximately 1 Gbps per cell in just five years to support the predicted mobile data growth.

Small cells (also known as femtocells) mounted on lampposts and connected via mesh networks are crucial in enabling operators to roll out the network in line with subscriber numbers, indeed they have been written into the LTE standard, but there are considerable challenges to overcome.

The first problem – how to cost-effectively send data between these small cells – is now effectively solved with the FCC backing the 60gHz band and allowing an increased permissible power for outdoor 60 GHz operations between fixed points (from +40 dBmi up to a maximum of +82 dBmi with +51 dBi gain antennas) provided a narrow antenna beam (under 0.4°) is used.

The following text therefore looks at the remaining four problems for network operators and outlines how backhaul small-cell equipment vendors can use the new FCC ruling and deliver backhaul more cost effectively.

2) Using the whole band

60 GHz backhaul equipment already exists, however, these offerings generally use FDD (frequency division duplex). This requires the use of guard frequency bands to separate transmit and receive frequencies, taking up 1-2 GHz (or 29%) of the usable frequency band for a single link.

Switching to TDD (time division duplex) architectures, like those used in WiFi and WiGig, allows the complete band to be used for both send and receive.

This has two additional advantages. Firstly, traffic allocated to up / downlinks can be dynamically adjusted to match the current traffic profile. Secondly, it eliminates the need for duplexers, which increase the cost (and small cell footprint); they also add significant loss in both the transmit and receive paths, with 2 to 4 dB loss being typical.

3) Optimising the baseband architecture for data rate and operational distance

Whilst WiGig may be used “out of the box” for 2 Gbps links, backhaul applications require the flexibility of trading data rate and operational distance.

The typical backhaul needs of an LTE small-cell base station are less than 1 Gbps; a link using a relatively low-order modulation, such as QPSK, can typically accommodate this.

Doing so is not only robust, it also allows you to future-proof the system, extending the data rate through the deployment of higher order modulation modes in future versions.

One alternative is to increase the radio link budget through the use of reduced channel bandwidth. For example, for each halving of the channel bandwidth the receiver sensitivity is improved by an additional 3 dB.

A flexible baseband architecture allows this scaling of frequency channel bandwidth thus enabling an increase in range, and providing a means of coping with differing operator scenarios.

4) Creating data packets for mesh networks

Data packetisation is controlled via the MAC function and it is not possible to simply use the standard WiGig MAC for LTE backhaul.

Indeed, data packetisation for LTE backhaul is particularly challenging and unlike standard P2P (peer-peer) networks, the wireless mesh networks used to transmit data between points add an extra level of complexity and each small cell needs to know if it is merely relaying – via the backhaul connection to another cell – or transmitting, via the mobile network to the phone.

For the time being there is no fixed standard – at Blu Wireless we are currently co-operating with several equipment vendors and operators to ensure our IP complies universally – but one solution is to use the OpenFlow standard as a MAC framework to define an industry-standard backhaul API.

5) Coping with the elements

LTE backhaul small cells will be positioned on lampposts and other street furniture and are therefore at the mercy of both the elements… and accidents.

The new FCC rules stipulate a narrow antenna beam width (under 0.4 degrees) and, as small cells for LTE backhaul transmit over distances of several hundred metres, even a position change of a fraction of degree will affect the quality of the mobile network.

Therefore, small cells need to not only be easy to install and align, they need to be automatically reconfigurable if moved or disturbed, and self-organising as the operator adds to the network.

Electronic antenna steering using phased array antenna (PAA) technology provides an ideal solution to these problems. Originally designed for military applications, this is now a mature technology and 60 GHz PAA technology is now becoming available at cost points compatible with the commercial constraints for small-cell backhaul. PAA technology also fits well with the emerging use of self-optimizing networks (SON) as SON could utilise PAA to dynamically steer antenna connections and thus re-configure network coverage for very high capacity hotspots.

About the author;
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HOW SMPS EVOLUTION HAS SPARKED A PSU DESIGN REVOLUTION

With banner statistics that proclaim DC/DC power-conversion efficiencies around 95% becoming another tick-box in the collective mindset, 30-plus years of taming “switchers” marks the end of the road for analogue evolution and the dawn of the digital revolution in PSU design.

Back in the tumultuous days of 1976 when “power to the people” advocated revolution over evolution in human affairs, Swedish engineer Magnus Lindmark kindled a PSU design revolution with a resonant circuit that increased the speed of switch-mode power supplies (SMPS) by an order of magnitude. Power bipolar-junction-transistors (BJTs) hampered switching speeds at a time that predates commercial use of power MOSFETs by several years, choking SMPS transient-response performance in particular. Yet six years after the US authorities published Lindmark’s patent in June of 1978, linear regulators continued to dominate the power-supply landscape with switchers normally serving only applications that demanded more than 250W. As an era of cheap energy supply burned itself out, heat dissipation remained linear's major issue with supplies routinely contributing 60% of their input energy toward global warming. As for low-power SMPS, cost and complexity restricted uptake to military and aerospace projects needing minimal bulk and power consumption. Exceptions include design classics such as 1972’s HP-35 pocket scientific calculator and the Apple II personal computer of 1977, both using switchers to efficiently generate multiple rails within minimal area.

Pre-Lindmark, a representative switcher ran at around 20 kHz leaving it with, perhaps, a mere 2 kHz of open-loop bandwidth to maintain regulation. But line-frequency power transformers and heat management measures are heavy consumers of aluminium, copper, and iron whose costs were continually rising. A shock price increase as demand outstripped supply contributed toward silicon vendors developing SMPS control ICs to rationalise design. In turn, the growth in SMPS uptake encouraged investments in silicon and design methods that saw linear power supplies relegated to local low-current provisioning, serviced by a people’s army of three-terminal regulators; or to niche low-noise applications in data-acquisition and audio/RF power amplification. Power MOSFETs arrived to solve multiple BJT issues — such as device matching — while furnishing greater efficiency and reliability, setting the course for a stream of evolutionary improvements to SMPSs that we now see on a plateau. Accordingly, another revolution is taking hold as analogue control methods finally cede to programmable mixed-signal technology, with “smarts” appearing — such as on-chip firmware that minimises power consumption by continually adapting a converter to its environment as it runs. Naturally, the output powertrain remains analogue and may even be identical between analogue and digital converters of similar output power.

Resonance boosts switching speed by an order-of-magnitude

While today’s SMPS designers expend massive efforts to extract an honest 1% improvement in virtually any parameter, early designs were lauded for efficiency metrics of as much as 80%, which was double that of many linear regulators. The path to maturity is way-marked by patent applications such as Donald A. Paynter’s “bridge-type transistor converter”, a self-biasing multivibrator (as shown in the figure) from US patent 4,097,773 of June 27th 1963.

More than a decade passed before Lindmark’s design circumvented fundamental issues with hard-switching at relatively high voltages by creating a resonant converter that soft-switches the power transistors at close to zero volts. At a stroke, this refinement mitigated electromagnetic compatibility (EMC) issues and relieved component stresses, to allow a maximum switching speed of around 200 kHz using BJTs of the period, together with a proportionate times-ten improvement in transient-response performance. Unlike today’s nonisolated low-voltage converters that may run at several MHz, a few hundred kHz remains good for many AC/DC front-ends and intermediate-bus converters (IBCs) regardless of switching method. This band hits a sweet-spot between the characteristics of everyday capacitors, magnetics, and power MOSFETs that with proven design delivers efficient and affordable power conversion that’s relatively easy to filter for EMC artifacts.

Unlike hard-switched topologies such as buck regulators and flyback converters that operate fixed-frequency pulse-width-modulation (PWM) control schemes, resonant converters depend upon switching-frequency changes to maintain regulation. Benefits should include making it easier to meet EMC regulations by distributing lower peak emissions across a wider bandwidth. Crucially, Lindmark’s switching cycle passes through zero, administering a sharp turn-off kick to cut power-switch losses that impact switching speed and efficiency. His revelations appear in US patent number 4,097,773 of June 27th 1978, and the continuation of this article (see link) reproduces one of the key diagrams from that patent application.
Why Total Jitter cannot be measured on an oscilloscope

By Ransom Stephens

Jitter is composed of a combination of random and deterministic signal impairments. Since RJ (random jitter) follows an unbounded distribution the combined total jitter distribution is unbounded.

Since trying to measure the peak-to-peak value of an unbounded quantity is silly at best and ill-defined and unrepeatable at worst, standards definitions in high speed serial technology typically cite a well defined peak-to-peak-like quantity called "total jitter defined at a bit error ratio." I call it TJ(BER): TJ(BER) because TJ depends on your choice of BER (bit error ratio).

Figure 1 is a drawing of a bathtub plot that includes the definition of TJ(BER). A bathtub plot is the graph of BER, the ratio of the number of bit-errors to the total number of bits transmitted, as a function of the time-delay, x, at which each bit is sampled, BER(x). BER is high near the crossing points of the eye diagram and drops as the sampling point moves toward the eye center—as you’d expect. TJ(BER) is defined as the amount of horizontal eye-closure at a given BER. The figure shows TJ(1E-12), which is the industry standard.

Figure 1 Bathtub plot, BER(x), showing the definition of TJ(BER) (graphic courtesy of Anritsu Corp.).

If you perform jitter analysis, you probably use an oscilloscope. Jitter can be analyzed on either a real-time or equivalent-time sampling oscilloscope, but TJ(BER) cannot be measured on an oscilloscope. You might be scratching your head and thinking, "But I read TJ(1E-12) off of my scope all the time."

Oscilloscopes estimate TJ(BER), but are incapable of measuring it. In fact, not only do scopes estimate TJ(BER), but they do so by extrapolating their measurements by a factor of about a million. Where interpolation consists of estimating what happens between two contiguous measurements, extrapolation is guessing what happens beyond your last measurement. The uncertainty of an interpolation is roughly the difference in the two measurements surrounding the interpolated point. The uncertainty of an extrapolation is...well, there’s no rule of thumb for the uncertainty of an extrapolation.

TJ(BER) can only be measured by a BERT (bit error ratio tester).

The reason that neither real-time nor equivalent-time oscilloscopes can measure TJ(BER) has to do with the tiny and huge numbers involved. To measure BER as low as 1E-12, you must analyze at least 1E13 bits.

It works like this. Say the true BER is exactly 1E-12. If you transmit 1E12 bits, there’s a 50% chance that you’ll get an er-
ror. If you transmit 1E13 bits, there's about a 30% chance you'll get an error. To get a 10% uncertainty in the BER, you need to transmit 1E14 bits. That's a lot of bits!

For a real-time oscilloscope to analyse the jitter of a hundred-trillion bits, you'll need at least ten samples for each bit to find the point where the edge crosses the slice threshold. To measure TJ(1E-12) a real-time oscilloscope would require a memory depth of about 1E15 bytes, a petabyte—a factor of about a million larger than is currently available.

The situation is worse for an equivalent-time oscilloscope. ET scopes under-sample signals, but aren't limited by memory depth. They acquire and acquire and just keep acquiring as long as they run, but they do it slowly. So slowly that a typical 100-Msample/second ET scope would take over two years to acquire enough data to measure TJ(1E-12).

You might be thinking that 1E14 bits is more than necessary. And, if you’re lucky, you’re right. We only really need a few billion over six trillion bits to measure TJ(1E-12) with around 10% accuracy (which is the best you can possibly hope for). The idea is to bracket rather than measure x-left and x-right. Since typical bathtub plots have such steep slopes below BER = 1E-9 or so, it's pretty easy to set the sampling point just inside x-left and let it run for 3E12 bits without getting an error and we're then assured to a 95% confidence level that the BER is less than 1E-12 at that x position.

Repeat the process on the right edge to constrain x-right. To get the outer constraint, use the standard fastBert scan technique down to about 1E-9. This is called the bracketing technique. Marcus Mueller and I wrote a paper about it several years ago and Agilent implemented it in software - the technique is not patented, by the way, so feel free to implement it yourself. While a scope still can't acquire six trillion bits, which would mean 60 trillion bytes at ten samples per bit period, 60 Terabytes is closer to reality than a petabyte.

The accuracy of any TJ(BER) measurement is limited by two factors. First, the quality of your BERT. Look for excellent error detector sensitivity, the minimum voltage swing that the error detector can decipher - 10 mV is state-of-the-art - and excellent timing linearity with quick pattern synchronisation. You'll need to be careful about whether you need a recovered clock to drive the error detector, too.

The second factor, I can't help you with. This is where the whole RJ, DJ, TJ, business might unravel. We typically measure TJ(BER) on signals with several jitter impairments on a repeating test pattern. The timing of jitter sources that correlate to the test pattern, such as ISI (inter-symbol interference) due to channel response, and those that are not correlated to the pattern, like PJ (periodic jitter) due to pickup of periodic noise and large RJ fluctuations, causes timing excursions of different amplitudes on different pattern transitions.

To have a chance of sampling the combined effects of ISI, RJ, and PJ we should analyse many repetitions of the pattern. If the test pattern is the standard PRBS31 (pseudo-random binary sequence with every permutation of 31 bits) and we want to repeat it 100 times, we need a lot of bits.
Capacitance at the input of the DC-DC converter plays a vital role in keeping the converter stable and playing a role in input EMI filtering. Large amounts of capacitance at the output of the DC-DC converter can provide significant challenges in the power system. A few simple techniques can be implemented within the power system to maintain an efficient and reliable design when powering highly capacitive loads.

Many loads downstream of the DC-DC converter need capacitance for proper operation. These loads can be pulsed power amplifiers or other converters that need capacitance at their inputs. If the capacitance at the load exceeds the value that the DC power system is designed to handle, the power system can exceed its maximum current rating at startup and during normal operation. The capacitance can also cause power system stability issues and lead to improper system operation and premature power system failure.

A few simple techniques can be implemented within the power system to maintain an efficient and reliable design when powering highly capacitive loads. Reducing the voltage rise time across the load capacitor at start up will keep the power system within its current rating, controlling the charge current into the capacitor during operation will keep the power system within its power rating and adjusting the control loop of the system will keep the power system stable and within system voltage ratings.

**Start up Considerations**

At start up, the typical DC-DC converter has a standard rise time set by the rise of an internal error amplifier reference. A discharged capacitor placed at the output of the converter will appear as a low impedance load. With this low output impedance, a few switching cycles of the converter can cause a change in voltage across the capacitor high enough to force the converter to exceed its output current rating. The capacitor can be pre-charged through a higher impedance path at the output of the converter. This high impedance element will limit the charge current into the capacitor until the capacitor is charged to a pre-defined voltage level. Once the pre-defined voltage level is reached, the high impedance path can be removed or shorted by a low impedance device such as an FET.

The converter can deliver its full rated current through this lower impedance path. When the FET shorts the impedance path, the full voltage of the converter is allowed to charge the capacitor. The turn-on time of the FET and the voltage differential between the capacitor and the converter voltage will determine the charge current needed to bring the capacitor to full voltage and thus it is important to set the pre-defined voltage level to a point where the FET turn on does not cause the converter to exceed its current rating. The block diagram in Figure 1 can be used to charge a capacitor to a preset voltage minimum. U2 controls the FET that shorts the impedance Z and the U1 circuit works in conjunction with U2 to set the turn on voltage and the load enable.

At start up the converter will see the capacitor as the load, in addition to the system loads following the capacitor. If the system load is demanding current from the capacitor during the high impedance pre-charge, the capacitor may not achieve the pre-set charge voltage. Many downstream loads to the DC-DC converter have an under-voltage lockout, under which they will demand little current. If the load does not have an under-voltage lockout above the pre set charge voltage then an external Enable should be used. If the load is resistive in nature, a series switch can be used to enable voltage to load after the capacitor is charged. Figure 2 shows the voltage and current of a system charging a 10 mF (10,000 µF) capacitor.

The article continues by looking at normal operating conditions, and factors affecting stability, when supplying substantially-capacitive loads.
Learn the essential capabilities for capturing elusive glitches with handheld scopes

See page 3
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**HINT**

Minimize spectrum analyzer measurement uncertainty by limiting the number of setup changes (such as RF attenuator or resolution bandwidth) you make from one test to the next. The fewer changes you make, the fewer uncertainties there are to contribute to overall measurement uncertainty.
Every experienced engineer and technician knows that infrequent events and glitches are the most challenging tasks in troubleshooting. Such a signal may be infrequent by design, or it might be a random, intermittent glitch caused by crosstalk or some other anomaly in the circuit.

In either case, capturing and analyzing these elusive events requires the right tools and the right techniques. If your troubleshooting takes you away from the lab bench or production line, you might find that the capabilities in today’s handheld oscilloscopes have everything you need for on-site troubleshooting.

**Catch events with glitch triggering**
Glitches can be extremely difficult to trigger on, particularly those that occur at random and unpredictable times. The glitch triggering feature in handheld scopes such as the Agilent U1610A/U1620A lets you define a tight window of signal parameters to find specific types of glitches. You can trigger on a positive- or negative-going glitch or on a pulse greater than or less than a specified width.

**Find the details with deep-memory zoom**
Glitch triggering combined with deep memory is a powerful troubleshooting combination. After you catch the glitch, you can scroll back in time and zoom into the signal data captured in deep memory to find the fault that caused it.

Of course, the more memory you have available, the longer you’ll be able to record data prior to the glitch—and the greater chance you’ll have of finding the root cause. In addition, you need to make sure your scope has a high enough sampling rate to provide sufficient resolution when you zoom in on the stored signal.

The U1610A/U1620A’s deep memory lets you capture up to two million data points (single channel in interleaved mode). Coupled with the benchtop-style 5.7-inch VGA display, this memory depth makes it much easier to explore the captured waveform at the “big picture” level and then zoom into the details when you need to. Figures 1 and 2 show the impact of having deep memory with high-resolution sampling.

Speaking of finding critical details, to troubleshoot with any success you need to be able to actually see the display well enough to read it, which hasn’t always been a sure thing in handheld instruments. The U1610A and U1620A offer three selectable viewing modes (indoor, outdoor, and night vision) giving you the flexibility to troubleshoot at any time, indoors or out.

**Making floating measurements, easily and safely**
Aside from glitch capture, on-site troubleshooting on motors, power units, and other devices often involves the need to make floating measurements, those without reference to a common ground.

The channel-to-channel isolation feature in U1610A and U1620A lets you perform floating measurements with CAT III 600V safety rating without reference to a common ground, while comparing the signals on the same display.

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---|---|---|---|---|---
U3401A | Dual display. Elegantly simple and affordable DMMs with basic capabilities | 4½ (U3401A) 5½ (U3402A) | N/A | DCV, ACV, DCl, ACI, 2-wire resistance and (4 wire resistance for U3402A), frequency, continuity, diode test | N/A
U3402A | | |
U3686B | A 5½ digit digital multimeter (DMM) with built-in 30 W power supply. Halves bench/ rack space needed for two instruments | 5½ | 26 | DCV, ACV, DCl, ACI, 2- and 4-wire resistance, capacitance, frequency, continuity, diode test, 30 W with four output ranges, OVP/DCP, auto scan/ramp and square wave generator | USB 2.0, GPIB
34450A | Faster measurement speed, ultra-bright OLED with dual display, and basic statistical tools | 5½ | 190 | DCV, ACV, DCl, ACI, 2- and 4-wire resistance, capacitance, frequency, continuity, diode test, temperature | USB 2.0, Serial Interface (RS-232), optional GPIB
34600A | Display DMM results in ways you never have before and measure with unquestioned Truevolt confidence | 6½ | 300 (34460A) 1,000 (34461A) | DCV, ACV, DCl, ACI, 2- and 4-wire resistance, frequency & period, continuity, diode test, temperature | USB 2.0, LAN (LXI Core) (34460A optional), optional GPIB
34401A | Industry standard for accuracy, speed, measurement ease and versatility | 6½ | 1,000 | DCV, ACV, DCl, ACI, 2- and 4-wire resistance, frequency & period, continuity, diode test | GPIB, RS-232, IntuLink software support*
34410A | Dual display. Highest throughput of benchtop DMMs, best choice for system use | 8½ | 10,000 (34410A) 50,000 (34411A) | DCV, ACV, DCl, ACI, 2- and 4-wire resistance, capacitance, frequency & period, continuity, diode test, temperature | LAN (LXI Core), USB 2.0, GPIB, IntuLink software support*
34411A | | |

*New DMM Connectivity Utility Software available.

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**The U1177A Infrared (IR)-to-Bluetooth® Adapter:** Enables Bluetooth connection to ALL Agilent U1200 Series handheld DMMs. Use with the complimentary Agilent apps, Mobile Meter and Mobile Logger, on your Android device to monitor and log data remotely and wirelessly (of up to 3 handheld DMMs).

<table>
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<tr>
<th>U1230 Series</th>
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<tr>
<td><strong>Counts</strong></td>
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<tr>
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<td>100 kHz</td>
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<td>30 mV to 1,000 V*</td>
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<tr>
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<td>1 µA to 10 A</td>
<td>500 µA to 10 A</td>
<td>300 µA to 10 A</td>
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<tr>
<td><strong>Battery life</strong></td>
<td>500 hours</td>
<td>300 hours</td>
<td>72 hours*</td>
<td>300 hours</td>
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<tr>
<td><strong>Additional features</strong></td>
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<td>Switch counter, harmonic ratio, dual and differential temperature measurements*</td>
<td>20 MHz frequency counter, programmable square wave generator*</td>
<td>Low pass filter, AC and/or DC voltage check, low impedance mode offset compensation*</td>
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</tbody>
</table>

**Connectivity**

IR-USB and Bluetooth

*S: Specification available on select models only.
DATA ACQUISITION/SWITCH UNITS
SPECTRUM ANALYZERS
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34907A multi-function
- 34905A/06A
- 34904A matrix
- 34903A GP switch
- 300 V, 20 actuator channels
- RF switches
- Up to 300 V, 16, 20, or 40 channels
- multiplexers
- 34901A/02A/08A

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- Free remote control PC software

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- DNL: -152 dBm typical, with preamp on
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- Sweep time: 2 ms to 1000 s
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- AM/FM, ASK/FSK demodulation
- Free remote control PC software

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- DNL: -148 dBm with pre-amp on
- RBW: 10 Hz to 3 MHz
- Sweep time: 2 ms to 1000 s
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- Free remote control PC software

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53220A
- 350 MHz universal frequency counter/timer, 12 digits/s, 100 ps

53230A
- 350 MHz universal frequency counter/timer, 12 digits/s, 20 ps

53200 Series
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- 53230A offers: 20 ps single-shot, burst microwave, and continuous gap-free measurements with time stamped edges
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<tr>
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<td>DSOX3AUTO</td>
<td></td>
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<tr>
<td>CAN symbolic/LIN trig/decode</td>
<td>DSOX2EMBD</td>
<td>DSOX3EMBD</td>
<td>DSOX4EMBD</td>
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<tr>
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<td>DSOX4COMP</td>
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<tr>
<td>USB signal quality test</td>
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<td>DSOX4USBQ</td>
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</tbody>
</table>

* 1 GHz models require DSOXPERFSO

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Agilent B2900A Series Precision SMU

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Max output range</td>
<td>210 V, 3.03 A (DC) / 10.5 A (Pulsed)</td>
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<tr>
<td>Best-in-class noise performance with filter</td>
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<tr>
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POWER CONVERSION TO SUPPLY MICROPPOWER APPLICATIONS AND THE INTERNET OF THINGS

The proliferation of wireless sensors supporting the “Internet of Things” has increased the need for small, efficient power converters tailored to tethered low power devices. Application scenarios, that would have appeared infeasible only a short time ago, include deriving full operating power from energy sources as scant as indoor lighting. Such applications typically feature low duty cycles and therefore require some form of energy storage; there are power-supply architectural choices to be made, even at this low level, to ensure the optimum combination of efficiency and availability of the end-product.

A generation of specifically-designed power conversion ICs is emerging to satisfy this need. For example, LTC3129 and LTC3129-1 are monolithic buck-boost DC/DC converters with an input voltage range of 2.42V to 15V. The LTC3129 has an output voltage range of 1.4V to 15.75V, while the LTC3129-1 offers eight pin-selectable fixed output voltages between 1.8V and 15V. Both parts can supply a minimum output current of 200mA in buck (step-down) mode.

Low power sensors can take advantage of the feature that both parts use zero current when disabled (on both VIN and VOUT), and a quiescent current on VIN of 1.3 μA when the power-saving Burst Mode operation is selected, suiting them to micropower and energy harvesting applications, where high efficiency at extremely light loads is crucial. A buck-boost architecture adds the capability to draw power from a variety of power sources.

Other key features include a fixed 1.2-MHz operating frequency, current mode control, internal loop compensation, automatic Burst Mode operation or low noise PWM mode, an accurate RUN pin threshold to allow the UVLO threshold to be programmed, a power-good output and an MPPC (maximum power point control) function for optimising power transfer when operating from photovoltaic cells.

A 3 × 3 mm QFN package and high level of integration ease placement into space-constrained applications. Only a few external components and an inductor, which can be as small as 2 × 3 mm, are required to complete the power supply design. Internal loop compensation further simplifies the design process.

3.3V converter from indoor light

The circuit in Figure 1 exploits the ability of the converters to start up and operate from an input power source as weak as 7.5 μW—making them capable of operating from small (less than 1in²), low cost solar cells with indoor light levels less than 200-lux. This enables such applications as indoor light powered wireless sensors, where the DC/DC converter must support an extremely low average power requirement, due to a low duty cycle of operation, from very low available power, while itself consuming as little power as possible.

In this case, the converters draw a meagre 2 μA of current (less in shutdown) until three conditions are satisfied: The RUN pin must exceed 1.22V (typical).

The VIN pin must exceed 1.9V (typical). VCC (which is internally generated from VIN but can also be supplied externally) must exceed 2.25V (typical).

Until all three of these conditions are satisfied, the part remains in a “soft-shutdown” or standby state, drawing 2μA.

This allows a weak input source to charge the input storage capacitor until the voltage is high enough to satisfy all three previously mentioned conditions, at which point the converter begins switching, and VOUT rises to regulation, provided the input capacitor has sufficient stored energy. The input voltage at which the part exits UVLO can be set anywhere from 2.4V to 15V using the external resistive divider on the RUN pin. With a RUN pin current of less than 1 nA typical, high value resistors may be used to minimise current draw on VIN.

In the application example shown in Figure 1, the energy stored on CIN is used to bring VOUT into regulation once the converter starts. If the average power demand on VOUT is less than the power delivered by the solar cell, the converter remains in Burst Mode operation, and VOUT remains in regulation.

If the average output power demand exceeds the input power available, then VIN drops until UVLO is reached, at which point the converter re-enters soft-shutdown. At this point, VIN begins recharging, allowing the cycle to repeat. In this hiccup mode of operation, VIN is positioned hysteretically about the UVLO point, with a VIN ripple of approximately 290mV in this example. This ripple is set by the 100mV hysteresis at the RUN pin, gained up by the UVLO divider ratio.

Note that by setting the converter’s UVLO voltage to the MPP (maximum power point) voltage for the chosen solar cell (typically between 70% to 80% of the open-circuit voltage), the cell always operates near its maximum power transfer voltage (unless the average load requirement is less than the power output of the solar cell, in which case VIN climbs and remains above the UVLO voltage).

To further optimize efficiency and eliminate unnecessary loading of VOUT, the converter does not draw any current from VOUT during soft-start or at any time if Burst Mode operation is selected. This prevents the converter from discharging VOUT during soft-start, thereby preserving charge on the output capacitor. In fact, when the LTC3129 is sleeping, there is no current draw at all on VOUT. In the case of the LTC3129-1, the VOUT current draw is sub-microamp, due to the high resistance internal feedback divider.

This article continues with consideration of operation with a back-up battery, and looks at the issue of where such a battery can be optimally placed relative to the energy source and the DC/DC.
You can create a parasitic capacitor on your board as long as two traces are in proximity. This capacitance is equal to the permittivity ($\varepsilon_R$ and $\varepsilon_0$) of the board material times the crossover area ($A$) divided by the distance ($d$) between the two traces.

$$C = \frac{\varepsilon R \varepsilon_0 A}{d} \quad \text{Eq. 1}$$

The dielectric constant ($\varepsilon_R$) of FR4, a glass epoxy used for PCBs, is from 4.4 to 4.8. We will use 4.7 in our calculation. The vacuum permittivity ($\varepsilon_0$) equals $8.84 \times 10^{-12}$ F/m. Figure 1 shows an example of two traces crossing on an FR4 PCB.

With a rise time of 10 nsec for a digital signal from 0 to 5V and a capacitance of 0.01 pF, the peak current is 50 µA. You can see that this is a fair amount of current, which flows into the second trace's impedance. If the second analogue trace's impedance is equal to 100 MΩ, this current creates a voltage spike of 0.5V. In the analogue world, this can be a very disruptive voltage spike.

A second scenario that creates board parasitic capacitance is where two traces, on the same layer, parallel each other. Figure 2 illustrates this circumstance. This capacitance is equal to the permittivity ($\varepsilon_R$ and $\varepsilon_0$) of the board material times the parallel length ($L$) times the trace thickness ($w$) divided by the distance ($d$) between the two traces.

$$C = \frac{\varepsilon R \varepsilon_0 L w}{d} \quad \text{Eq. 3}$$

Again, let’s use 4.7 for the dielectric constant ($\varepsilon_R$) of FR4 PCB and the vacuum permittivity ($\varepsilon_0$) of $8.84 \times 10^{-12}$ F/m. A typical application board where this may occur is where the parallel length ($L$) is equal to 5 cm and the distance between the traces is 0.5 mm. If you use Equation 3 for the Figure 2 dimensions, the capacitance between these traces is approximately 0.01 pF.

These are two examples of how to build low-cost capacitors on your PCB. Unfortunately, these capacitors, combined fast-switching speeds and high-impedance analogue lines to create a disaster. For instance, imagine that your switching speeds are sub-nanoseconds long and your analogue lines are high impedance, such as the input to an amplifier. You will see some severe signal integrity problems arise!

So what do you do? Generally, separate your digital activity from your analogue activity on the board. By separation, I do not mean put these activities in separate layers. Decrease these parasitic capacitor sizes as much as possible in Figure 1 by increasing the distance between the cross-over traces. If you have a Figure 2 circumstance, decrease the length ($L$) of your parallel traces, increase the distance, $d$, between these parallel traces. Remember, $d$ is in the denominator of the equation.

Another solution for the problem in Figure 2 is to slip a ground trace between the two traces. See Figure 3 for this solution.

Bonnie Baker is a senior applications engineer at Texas Instruments.
Measurement systems  

Every application of measurement, including those not yet invented, can be put into one of three categories or some combination of them: monitoring of processes and operations; control of processes and operations; and experimental engineering analysis. In real-time control applications, a process is subject to disturbances and ageing, and its model parameters are not exactly known.

In the open-loop system, this results in a changing and inaccurate output. However, a closed-loop system senses the change in the output and attempts to correct the output. The sensitivity of a control system to parameter variations and disturbances is of prime importance. A primary advantage of a closed-loop (feedback) control system is its ability to reduce the system’s sensitivity. As the loop gain is increased, the sensitivity of the closed-loop control system to changes in the process and controller decreases, but the sensitivity to changes in the measurement system becomes −1. In real-time, closed-loop-control applications, the measurement system must be accurate, fast, and stable.

Inputs to a measurement system, Figure 1, consist of: desired inputs ID (quantities that the system is specifically intended to measure); and interfering inputs IF (quantities to which the system is unintentionally sensitive). FD and FI are input-output relations, i.e., the mathematical operations necessary to obtain the output from the input. Then there are modifying inputs IM (quantities that cause a change in FD and/or FI). FM,D and FM,I represent the specific manner in which IM affects FI and FD, respectively. There are several methods to correct for the modifying and interfering inputs. One method is filtering and a most interesting application of filtering is sensor fusion, the creation of an ideal virtual sensor from two less-than-ideal real sensors. It is used in self-balancing robots to give a fast and accurate measure of the robot tilt angle. The sensor fusion scheme with digital implementation is shown in Figure 2.

A two-axis accelerometer gives a fast measure of the accelerations of the robot in the balancing plane, including the acceleration due to gravity from which the tilt angle can be obtained. A single-axis rate gyroscope gives a fast and accurate angular measurement of the robot in the balancing plane. The gyroscope can be integrated to give the tilt angle, but if the gyroscope does not read perfectly zero when stationary (and it won’t!), the small rate will keep adding to the angle until it is far away from the actual angle. A low-pass filter, digitally implemented, applied to the accelerometer filters out short-duration accelerations leaving only the long-term acceleration due to gravity. There will be a time lag in the accelerometer reading due to filtering. A high-pass filter, digitally implemented, applied to the gyroscope filters out the bias error in the integrated angle. The two filtered signals are added together to give a fast, accurate estimate of the tilt angle with much less time lag than the low-pass filter alone.

Measurement systems play a critical role in all real-time applications. Understanding how the various inputs combine to affect the desired measurement, along with techniques to mitigate undesirable effects, is essential for all engineers.
Design teams building high-speed, next-generation network communications equipment suffer under the constraints imposed by memory. Some design solutions use only on-chip memory which is inherently limited in capacity and competes with silicon area that could be otherwise used for computation or other functionality.

More complex applications require external memory and at the processing rates available today need the highest possible random access rate to that memory. Traditional memory interfaces are a burden to performance because they are plagued by slow speeds, lengthy latency, and high pin counts. As a result, conventional design approaches to implementing external memory have already reached the point of diminishing returns.

Serial protocols & standards break the I/O bottleneck

Consider any modern System-on-Chip (SoC) available today and you will see nearly all the interfaces are serial, except for that to traditional memory ICs. Going forward, the transition to serial memory has already begun and decisions need to be made regarding which serial interface protocols to support. Any interface can be delineated into its physical layer or PHY, transport protocol or PCS, and transaction layer or the command set. Standardisation can take place on each level, independently.

Regarding the serial PHY; the industry standards group, the Optical Internetworking Forum (OIF), published the Common Electrical Interface I/O (CEI) standards including CEI-11 in September 2011 [Ref. 1]. Standards development groups such as OIF require three to five years to develop channel models, set clocking and jitter budgets, determine electrical signal coding, and encourage the development of the ecosystem. As a result, these standards are [now] being adopted for a broad range of applications.

In fact, three serial memory interface protocols have adopted the CEI-11 physical definition: the GigaChip Interface (GCI) [Ref. 2], the Interlaken Look-Aside (ILA) [Ref. 3], and the Hybrid Memory Cube Interface (HMC) [Ref. 4] as indicated in Figure 1. Design teams can expect these protocols to also conform to the CEI-25 standard in the future. Each of these protocols targets different applications and markets as outlined in Table 1.

Designers therefore do not need to develop three different interface solutions to meet multiple use cases. Instead, host processors can incorporate two or more protocols running on the same physical layer. The interface need not be limited to memory but could also be used for general serial IO, giving the ultimate flexibility to the system designer in addressing a broad range of market applications.

Although it is possible to multiplex the protocols, a close look reveals distinct performance differences. Protocols leveraged from other applications result in unnecessary overhead and latency when used in point to point applications, such as a high performance memory interface. It may be necessary in the near term to include all three serial protocols on the SoC processor in order to support performance capabilities and devices from different manufacturers. If a customer wants to consolidate to two or one interface only GCI offers high efficiency for all the memory access patterns used on high performance networking line cards.

Networking applications tend to have three types of memory access patterns, depending on the function being performed. These are discussed in the continuation of this article, follow the link below.

Also see, by this author; “Serialised memory interface gains momentum”

Complete article, here
VALIDATION AND ANALYSIS OF COMPLEX SERIAL BUS LINK MODELS

Faster signalling speeds and shrinking geometries have created the need for robust serial data link applications to support modelling, measurement, and simulation of live waveforms on a real-time oscilloscope. Designs are evolving to address these challenges with advanced equalisation techniques at the transmitter and receiver. Smaller form factors make signal access more difficult resulting in non-ideal probing points. This can lead to loss and reflections on the acquired signal due to impedance discontinuities that would not be present at the ideal measurement location.

Serial data link analysis applications allow the user to load circuit models for the measurement circuit, which includes the test and measurement fixtures and instruments used to acquire waveforms from the DUT. This allows the loss and reflections caused by fixtures and test equipment such as the probe and scope to be de-embedded from the acquired waveforms. De-embedding these effects improves the accuracy of measurements and can make the difference between passing and failing a test. In addition, link analysis applications allow the user to define the simulation circuit by loading channel models for the serial data link system in order to evaluate performance without the need for actual link hardware to be present.

A typical usage scenario would be to acquire waveforms through fixtures from an actual transmitter circuit that is to be evaluated. This allows for observation of waveforms out of the transmitter with the measurement circuit removed, and with an ideal load simulated. Also, the serial data link simulated models can be connected to the transmitter (TX) to evaluate the signal at the far end and the receiver (RX) model can be modelled using CTLE equalisation, FFE/DFE equalisation, or the RX IBIS-AMI model. The signal can then be simulated at any test point within the link resulting in the output of live waveforms that can be used in other applications for to measure signal quality, including jitter and eye diagram analysis.

In an example of such a modelling setup, the system would acquire input waveforms from an oscilloscope and apply a transfer function to the acquired signal to obtain test point waveforms. These test points allow the user to view the waveform at any point in the link and appear as live waveforms on the oscilloscope display.

Ensuring adequate test margins

With data rates moving to from 5 Gb/sec to 10 Gb/sec and beyond, every picosecond and millivolt count to ensure that adequate margins are met. The goal is to measure the DUT (device under test) and not the test equipment, fixtures or cables that are used to acquire the signal. The act of removing the effects of an SMA cable, as an example, can result in a significant improvement in the margin of the device. The higher the frequency of the signal, the more pronounced the results become.

In the example that generated the waveforms in the figure, an 8 Gb/sec PRBS7 signal is acquired with a SMA cable through SMA connectors soldered directly to the test board. The goal is to remove the effects of the SMA Cable from the test board. These effects include the loss through the cable and any reflections due to impedance mismatches in the cable and the cable connections. Before the cable effects can be de-embedded the measurement circuit must be completely characterised. This includes knowing the TX output impedance, cable model, and the input impedance of the receiver, which is the oscilloscope. For simplicity, it is assumed that both the TX output and RX input impedances are nominal 50Ω. Using a TDR or VNA, S-parameter models of the SMA cable can be obtained and used in the de-embedding process.

Using serial data link analysis software, the S-parameter of the cable is loaded into the de-embed block. The end result will be the waveform with the SMA cable removed. The reflection and transmission terms can quickly be verified using plots as shown in the Figure. The reflection coefficients are represented by S11 and S22 and the transmission by the terms S21, S12. For passive circuits the forward and reverse transmission terms are identical as shown in the example in the Figure: if they are not, then there are errors in the measurements.

In this example, each leg of the SMA cable is represented by two separate 2-port S-parameter models. Though the cable only has 1 dB of loss at the fundamental frequency of 4 GHz, this still equates to about a 10% reduction in the high frequency content of the signal. It can also be easily observed that as the frequency of the signal increases the loss also increases and thus the impact the cable has on the margins of the DUT.

In the continuation of this article, the author adds time-domain measurements and expands on the detailed de-embedding process and the software that supports it.
The SCR is a switching semiconductor device, whose theoretical basics were published by Moll et al. in 1956 (Ref 1). Although lower power parts have almost disappeared from the contemporary switching scene – being replaced by high-voltage BJTs, MOSFETs, and IGBTs – they still have no competition in the megawatt-switching area. 2 kA, 1.2 kV SCRs are used in locomotive drives, to control electrical furnaces in aluminium production plants, etc.

An SCR is a four-layer semiconductor device with a transistor equivalent shown in Figure 1a. The device is in the off-state until a positive current pulse is fed into gate 1. After that, the four-layer structure between anode and cathode turns on, and the gate current is no longer needed. Here also, the base of Q2 can be used to turn on the SCR, but monolithic SCRs usually have cathode-referred gates only.

A more realistic transistor model contains base-emitter resistors for both PNP and NPN transistors, as in Figure 1b. Thus, an undesired turn-on by leakage currents of Q1 & Q2 is avoided, and the gate current has a defined value of:

\[ I_{G1} \geq \frac{V_{BE1}}{R_{B1}} \]

One limitation of SCRs in general is that if the risetime of anode voltage exceeds a critical rate, the SCR is turned on despite zero gate current. This anode voltage is called the commutation voltage, and it appears across switched inductive loads, when anode current goes to zero and drops below the hold level. The energy accumulated in the inductance tends to create an abrupt rise of anode voltage at that point. A commutation voltage also occurs when switching resistive loads by a combination of at least two SCRs, connected in a form of an analogue multiplexer, where an SCR being turned on exerts an abrupt rise of anode voltage at another SCR.

For the circuit of Figure 1b, the critical value of slope of commutation voltage is:

\[ S_{V_{crit}} \approx \frac{V_{BE0}}{(C_{CB01} + C_{CB02})R_B} \] 

Where \( V_{BE0} \approx 0.7V \), the typical voltage at which a silicon transis-

Figure 1. A basic SCR-like structure (a), gets well-defined values of gate and hold currents (b), and vastly improved immunity against undesired turn-on at steep rise of anode voltage (c).
The purpose of this Design Idea was to improve reliability, add new features, and replace a latching power switch with a momentary one. The features are:

- The switch has foolproof protection against too frequent switching, which can be harmful for many applications.
- It can handle significant power because manual control and switching are separated.
- If an unexpected power outage occurs, the switch disconnects and remains off after power returns.
- A unit can switch itself off.

The control button BUT1 requires normally open and normally closed contacts, which must not be closed simultaneously.

Initially, while the button is not pressed, the switch is opened because relay K1 is deactivated. The normally-open contacts of the relay and the button are the only components under voltage in this state.

When the button is actuated for the first time, the capacitor C1 is charged through D1 & R1, and relay K1 is activated, closing its contact pair SK1. The relay from now on is powered via D4 and R4.

When the button is released, the NC contacts allow C2 to charge to about one-half of the mains voltage through R2 & D2. This prepares the switch for subsequent shutdown when the button is pressed again. Q1 is on and Q2 is off.

With the next press of the button, both transistors change their state, and the discharge current of C2 triggers SCR D6, de-energising the relay and disconnecting the load. Due to the latching action of the SCR, this state cannot be reversed by any subsequent actuation of the button while C1 is not discharged.

Releasing the button returns the circuit to its initial state.

LED D7 and protection diode D8 are embedded in the button.
Modern LEDs are bright enough with a current in the range of 0.1 - 0.2mA, so despite the relatively high voltage, the total power consumption for the illumination is about 5 - 10mW or less.

An optional opto-thyristor D11 adds the ability for a powered system to be switched off from within the system.

Resistor R1 protects the button’s contacts from an inrush current. The constant R1C1 moderates the turn-on time.

The capacitor C3 should be placed close to D6 to prevent false triggering due to EMI.

Resistors R9 & R10 limit the current through LED D7. There are two resistors for mains of 220V (to reduce the voltage on each resistor). For mains of 110V, R9 alone can be used.

The value of R5 depends on the resistance of the relay coil (r) and value of Vin.

Either SCR should withstand a peak current of: \( \frac{V_{in}}{R_5} \) and its off-state voltage should be not less than: \( \frac{V_{in} \times r}{R_5 + r} \)
This Design Idea drives the ±20 mA current loops that are often used to control two-way proportional pneumatic or hydraulic servo valves in high power robotics applications. Most current drivers are capable of driving unipolar outputs only. Bipolar current drivers often require negative supply voltages.

The circuit operates from a single supply, uses dual or quad components in very small packages, and takes up very little board space. A set of four drivers may be built in less than two square inches of printed-circuit-board area, including connectors.

Opposing output MOSFET pairs Q1A/Q3B and Q1B/Q3A are enabled to send either positive or negative current to the valve. Current sense resistor R3, connected to the output MOSFET source leads, feeds back the current to wide operating range rail-to-rail I/O op-amp U1. Rs1D, C1, and U1A form an integrating amplifier that turns on the MOSFET output stage in proportion to the voltage applied at the I_CONTROL input.

The current output range is set by resistor divider R1 and R2 in conjunction with sense resistor R3:

\[ I_{out} = \frac{V_{in} \times R_2}{(R_3 \times (R_1 + R_2))} \]

Setting the DISABLE input high turns on Q2A and forces the control voltage into integrator U1A to zero volts, resulting in zero current output. When the POLARITY input is low, Q4B’s gate goes high, forcing Q1A and Q3B off. Q4A’s gate is low, allowing Q1B and Q3A to be controlled by U1. When the POLARITY input is high, Q4A’s gate is high, forcing Q1B and Q3A off. Q4B’s gate is pulled low, allowing Q1A and Q3B to be controlled by U1.

The driver output voltage is limited by the op-amp supply voltage. The maximum drive voltage with the shown values is:

\[ V_{outU1} - V_{thMOSFET} - V_{Rsense} = 12V - 3V - (20mA \times 36\Omega) \]

\[ = 8.3V \]

Notes: Resistor pack RS1 is Panasonic EXB-V8V103JV, all MOSFETs are Fairchild duals, type NDC7002N.
ST attacks MCU dynamic power with 90-nm process, voltage scaling

**STM32F4 MICROCONTROLLERS ARE THE FIRST IN WHAT**

STMicroelectronics is calling its STM32 Dynamic Efficiency range; ST says it combines multiple technologies to offer the best balance of dynamic power consumption and execution performance, while boosting feature integration. Technologies include a feature called ART Accelerator, a prefetch queue and branch cache. This allows zero-wait-state execution from flash memory for performance of 105 DMIPS (285 CoreMark) at 84 MHz and helps achieve RUN current down to 128 μA/MHz. STOP mode current is 9 μA at 1.8V. Devices integrate up to 512 kByte of flash and 9 kByte SRAM in a 3.06 x 3.06 mm chip-scale package. Peripherals include three 1 Mbit/sec I²C ports, three USARTs, four SPI ports, two full-duplex I²S audio interfaces, USB2.0 OTG Full-Speed interface, SDIO interface, 12-bit 2.4Msample/sec 16-channel ADC, and up to 10 timers.

**40 GHz handheld cable and antenna analyser**

**ANRITSU’S MICROWAVE SITE MASTER S820E IS CLAIMED as the first handheld cable and antenna analyser with frequency coverage up to 40 GHz. With dynamic range of 110 dB up to 40 GHz, the instrument offers in-the-field performance typically only achieved with a benchtop instrument; frequency resolution of 1 Hz provides maximum frequency flexibility for users. Sweep speed is 650 μsec/data point; directivity is the highest available in a handheld analyser for maximum field accuracy. It also features RF immunity of +17 dBm. Designed for measuring coaxial and waveguide systems, Site Master S820E conducts all key one-port measurements, such as return loss, VSWR, cable loss, DTF, phase, and Smith Chart. Users can also conduct two-port transmission measurements and two-port cable loss tests with the Site Master S820E.**

ADCs for medical, industrial measurements

**THE 1-CHANNEL SAR ADC ADS8881 FAMILY OF 12 PARTS includes ultra-low power 18- and 16-bit SAR ADCs with speed options ranging from 100 ksamples/sec to 1 Msamples/sec. Most of the new ADCs provide an input common-mode range that is 20-times wider than other devices. Analogue supply voltage range is 2.7 V to 3.6 V, which enables direct operation from a Lithium-Ion battery. Digital supply voltage range is 1.65 V to 3.6 V, meeting most microprocessor supply requirements. The 1-Msample/sec SAR ADCs consume 5.5 mW of power at 1 Msamples/sec and 55 µW at 10 ksamples/sec, making them suitable for pulsed DC measurements in portable medical and heat-sensitive automated test applications. Six accompanying TI Precision Designs reference design circuits provide theory, simulation, calculation, and design methodology.**

**Bosch “Fusion” 9-axis orientation sensor**

**THE BNO055 FROM BOSCH IS THE FIRST IN A FAMILY OF Application Specific Sensor Nodes (ASSN) implementing an intelligent 9-axis “Absolute Orientation Sensor”, which includes sensors and sensor fusion in a single package; it is available from distributor Rutronik. The BNO055 is a System in a Package (SiP), integrating a triaxial 12-bit accelerometer, a triaxial 16-bit gyroscope with a range of ±2000 degrees per second, a triaxial geomagnetic sensor and a 32-bit microcontroller running the company’s BSX3.0 FusionLib software. At 5.2 x 3.8 x 1.1 mm, it is smaller than comparable discrete or system-on-board solutions and intended for augmented reality, more immersive gaming, personal health, fitness and well-being, indoor navigation and any other application requiring context awareness.**
Precision op amp for industrial measurements

TEXAS INSTRUMENTS CLAIMS TO HAVE THE FIRST 36-V rail-to-rail input and output (RRIO) operational amplifier (op amp) to achieve precision offset voltage and drift without using auto-zero techniques. The OPA192 achieves stable offset voltage drift over the full specified temperature range, which eliminates the need for system level calibration. It provides 5-µV offset voltage and 0.2-µV/C offset drift over temperature without the use of internally clocked auto-zero techniques, which increases the accuracy of industrial sensor signal conditioning. RRIO enables maximum input dynamic range for precision high-voltage measurement in industrial automation and control applications. 60-mA output current drive and 1-nF capacitive-load drive provide system stability for high-voltage buffers and multiplexed data acquisition.

Rapid charge interface for faster battery charging

DIALOg SEMiCONDuCTOR HAS COLLABORATED with Qualcomm Technologies to develop higher efficiency rapid smartphone charging; the Qualcomm Quick Charge 2.0-compatible AC/DC adapter enables up to 88% efficiency for high power density, rapid charge power supplies up to 40W. The iW620 rapid charge interface IC resides on the secondary side of the AC/DC charger power supply and works with Dialog’s iW1760 PrimAccurate primary-side digital pulse width modulation (PWM) controller. Efficiency as high as 88% enables the higher power density needed for smaller form-factor fast charging adapters. Quick Charge 2.0 is a proprietary protocol from Qualcomm Technologies, for charging smartphones, tablets and other mobile devices up to 75% faster than conventional USB charging technology. Dialog’s Quick Charge 2.0 rapid charge AC/DC adapter solution delivers high efficiency up to 83% without the need for a synchronous rectifier that Dialog says is required by competing solutions. If a synchronous rectifier is used, it can achieve higher efficiency of up to 88%. The iW620 supports Quick Charge 2.0 High Voltage Dedicated Charging Port (HVDCP) Class A (5V, 9V, 12V output) applications and, with the iW1760 primary-side digital PWM controller, it provides fast voltage transition and low no-load power consumption of under 100 mW.

Raspberry-Pi NFC expansion board

FROM DISTRIBUTOR FARNELL ELEMENT14, THE EXPLORE-NFC expansion board implements external user interfaces for industrial and consumer devices that meets NFC compliance with Reader mode, P2P mode and Card Emulation standards. Based on the PN512 NFC solution from NXP Semiconductors, the board has an integrated high performance antenna and is supported by a software package (libnfc) while offering a flexible SPI interface. Applications for NFC include contactless payment, meter readings, and loyalty cards. Connecting to the Raspberry Pi, it offers compliance with all three NFC modes (Reader, P2P and Card Emulation); the reader mode supports all four NFC tag types and NXP’s MIFARE command set; a flexible interface selection (SPI or I²C), and it includes a software stack for SPI Integrated high performance RF antenna. It has NXP’s MIFARE Ultralight NFC card (NFC forum tag type 2) for quick-start development.

RS’ free PCB software links to DesignSpark Mechanical

DISTRIBUTOR RS COMPONENTS HAS RELEASED VERSION 6.0 of DesignSpark PCB, its software for schematic capture and PCB layout, adding three of the most-requested new features: Simplified export to DesignSpark Mechanical, Cross Probe, and Custom Shortcuts. RS launched DesignSpark Mechanical in September 2013, with which users can design the mechanical elements of their products with a free-of-charge tool from the DesignSpark suite. DesignSpark PCB Version 6.0 comes with simplified IDF export dedicated to DesignSpark Mechanical. The Cross Probe (X-probe) functionality in Version 6.0 further speeds up the design process by allowing instant referencing between the schematic and the PCB-design views within the software. The new Custom Shortcuts functionality in Version 6.0 allows more customisation flexibility within the user interface.
Linux-based automotive infotainment

MENTOR GRAPHICS HAS ISSUED THE LATEST RELEASE of its Mentor Embedded Automotive Technology Platform (ATP) for Linux based in-vehicle infotainment (IVI) system development, bringing responsive user interfaces or HMIs, similar to those seen in consumer electronics devices, with the new graphics development and optimisation functionality added to this GENIVI 5.0 compliant release. By combining ATP with the recently announced Mentor Embedded Hypervisor, automotive OEMs can integrate functionality such as device connectivity, on emerging infotainment hardware system-on-chip (SoC) architectures while maintaining secure separation for critical functionality. The new release includes graphics framework support for X11 and Wayland, GPU support and an instrumented package for QT 5.0 that includes the visual and interactive analysis of UI smoothness, start-up time, latency and QML activity.

35A “Power Block” DC-DC converter module

MURATA’S LATEST ADDITION TO ITS OKLP RANGE OF “Power Block” products is the OKLP-X/35-W12-C, a 35A Power Block solution. This Power Block concept sits between a discrete Point-of-Load (PoL) design and that of a complete non-isolated buck converter module. The Power Block is essentially a non-isolated buck converter without the PWM controller. The OKLP-X/35-W12-C power block measures 25.4 x 12.7 x 11.1 mm and has a typical efficiency rating of 94%. Input voltage is a nominal 12 VDC and can accommodate the range of 7 to 13.2 VDC. When coupled with ZMDI’s ZSPM1035 single-phase digital PWM IC controller family, the combination of the ZSPM1035 and the 35A Murata Power Block provides a ready, tested, and preconfigured 35A point-of-load solution. Designers have access to a full downloadable construction kit that includes step-by-step instructions and a software wizard. Mouser Electronics as distributor for both ZMDI and Murata Power Solutions will be able to provide the ZMDI controllers, GUI interface, Murata’s OKLP and Evaluation Boards.

4-wire resistive touch panels with gesture

ROHM SEMICONDUCTOR’S BU210XX SERIES OF 4-WIRE resistive touch panel controller ICs come in a variety of package options and include a 8-bit or 32-bit CPU for 2-point gesture detection and a calibration function for enhanced flexibility and reliability. Automotive-grade types are available. Proprietary technology and compact design enable component reduction and easier, user-friendly operability such as gesture input when wearing gloves. The resistive touch method typically provides 1-point detection operation using a stylus/pen or for simple button selection. However, ROHM has developed and mass-produced 2-point detection controller ICs that are market-proven and have been widely adopted in automotive applications such as displays for audio and car navigation systems.

DC regulators in under-3-mm profile

EXAR’S XRP9710 AND XRP9711 ARE MULTI-OUTPUT, synchronous step-down, programmable power modules that claim highest power density and lowest profile at 2.75 mm with 5V - 22V inputs. Both devices provide two fully integrated regulators with MOSFETs, inductors, and internal input and output capacitors in a 12 x 12 x 2.75 mm package that support loads up to 6A each. The XRP9711 also offers two controller outputs that are each capable of driving loads up to 30A: two fully integrated channels and two controller outputs. The XRP9710 and XRP9711 are complete system power solutions that enable telemetry, reconfiguration and fast time to market in a small footprint without sacrificing performance. These power modules offer full control via a SMBus-compliant I2C interface allowing for advanced local- and remote-reconfiguration, full performance monitoring and reporting, as well as fault handling. Their output voltages can be programmed from 0.6V up to 5.5V without requiring any external components.
250 MHz to 12.4 GHz fractional/integer-N PLL

MAX2880 is a high-performance phase-locked loop (PLL) capable of operating in both integer-N and fractional-N modes. Combined with an external reference oscillator, loop filter, and VCO, the device forms an ultra-low noise and low-spur frequency synthesiser capable of accepting RF input frequencies of up to 12.4 GHz. It comprises a high-frequency and low-noise phase frequency detector (PFD), precision charge pump, 10-bit programmable reference counter, 16-bit integer N counter, and 12-bit variable modulus fractional modulator. The device is controlled by a 3-wire serial interface and is compatible with 1.8V control logic. It comes in a 4 x 4 mm, 20-pin TQFN package, and operates over an extended -40 to +85°C temperature range.

8-mm-sq, low-power 802.11b/g/n Wi-Fi modules offer ease of integration

ECONAiS INC. CLAIMS TO HAVE THE SMALLEST-available, most easily integrated, and lowest standby power single chip 802.11b/g/n Wi-Fi System In Package (SiP) modules for the Internet of Things. EC19D incorporates the newest Wi-Fi 802.11b/g/n standards and features to give designers a full array of options for embedding the module in their designs. Features include: Wi-Fi Direct, ProbMe configuration, full TCP/IP stack, HTTPS/SSL, DHCP Client/Server, WPS, legacy Wi-Fi Client and SoftAP modes with WPA/WPA2 support, Serial to Wi-Fi, and Cloud Service Support. The modules measure 8 x 8 mm. ProbMe is a proprietary configuration method which enables any Wi-Fi device to configure the EC19D module without the need of any application.

Optical image stabilisation MEMS gyroscope

STMICROELECTRONICS HAS INTRODUCED A 2-AXIS gyroscope optimised for optical image stabilisation in smartphones and digital still cameras. With dimensions of 2.3 x 2.3 x 0.7 mm, the L2G2IS can be integrated into the next generation of stabilised camera modules, where the dimensions of the components are critical. At a size 50% smaller than the previous generation by area and 60% smaller by volume, the L2G2IS still provides the high performance demanded by the applications and consumers. Key technical features of the new device include ±100 dps / ±200 dps full-scale range, 3- and 4-wire SPI interface, and integrated low- and high-pass filters with selectable bandwidth. The L2G2IS operates with a supply voltage range of 1.7V to 3.6V. Samples of the L2G2IS gyroscope are available now and pricing is $1.70 (1000).

High-speed connectors pass 25 Gbps

MICROSPeed FAMILY CONNECTORS FROM ERNI Electronics are initially specified for data rates of up to 20 Gbps (using differential pairings). Current measurements and simulations now prove that, with suitable design criteria and layout (-2 dB insertion loss, 5 mm board-to-board spacing), data rates of more than 25 Gbps are possible. This in turn allows extremely fast board-to-board connections with distances of 5 to 20 mm to be realised. The modular, shielded connectors with 1.0 mm pitch are available as a two-row version with 50 pins for operation in the temperature range -55°C to +125°C. In addition to right-angle variants in the two-row design and robust blind-mate versions, seven-row versions with 91 and 133 pins respectively are also available.
One small step for synchronisation

I was once asked to look at a high-voltage signal generator schematic. It was to be used for a dielectric-paper photoprinter being designed for the Associated Press by EG&G. The circuit’s output was to be 800V variable-duty-cycle rectangular wave at 10 kHz. The schematic, with stacked high-voltage transistors, reminded me of a mistake I made at my first engineering job, helping to design the Apollo navigation computer at the MIT Instrumentation Lab.

The job was insanely fascinating, with astronauts visiting the lab and occasional trips to Cape Canaveral to admire the rockets, but it also taught me the advantages of synchronisation.

My first assignment was designing the schematic of the power supply for the electroluminescent display. The supply was to generate several hundred volts of 400 Hz sine wave at high efficiency. The load was mostly capacitive and changed considerably depending on the displayed numbers.

Inexperienced but enthusiastic, I built a Wein bridge oscillator and hooked it up to a class B linear amplifier with a transformer for the voltage boost. I figured that a square wave drive and resonating a series inductor with the load would give me much higher efficiency, but as the load capacitance changed considerably depending on how many segments were illuminated, that didn’t work. But I thought it was decent, except that brightness change with load was visible. I added a feedback circuit to sense output voltage and fix the brightness problem. The floor under the lab bench was littered with dead transistors, but maybe bigger transistors would fix that minor issue.

I confidently presented the design to management, who patted me on the head and began my education.

"Kid," he said, "there’s two things: One is synchronisation. We’d like the Apollo crew to have a decent chance of surviving the trip, so we like to test the entire electronic system in all possible modes. If we have lots of unsynchronised processes, it takes a very long time to do the testing. So we like everything to be synchronous."

"Piece of cake, sir," I responded. "I’ll run a simple phase-lock loop off the master oscillator."

"Not a bad idea; or just a counter for even more stability," he replied. "The second thing is the efficiency – we should be able to do better. And the third thing, you’re using a whole lot of parts."

I was once asked to look at a high-voltage capacitor tester schematic. I confidently presented the design to management, who patted me on the head and began my education.

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Along with decreased test time, I found that a system with multiple asynchronous processes tended to have crosstalk that looked like random noise. A board with analogue inputs to an ADC picked up this noise and degraded the ADC output signal. But with everything synchronous, including the ADC clock, this noise source disappeared.

So when I saw the signal generator schematic a few years later, having successfully participated in the very exciting Apollo 11 moon landing, I was ready. I used a synchronous clock driving a flyback circuit, with a transformer primary on the 15V rail generating 80V 5μsec positive pulses that were amplified to 800V at the 10X transformer secondary. The positive pulses charged the load capacitance up to 800V through a low-capacitance high-voltage diode string, and the load capacitance retained the voltage when the pulse terminated.

A similar circuit with the output polarity reversed then generated a similar but time-delayed negative pulse that discharged the load to -800V through another diode string. With no high-voltage transistors, the circuit worked reliably and the printer made good wire photos.

I learned two things from this experience: keeping the system synchronous improves noise performance as well as speeding test time; parts that you don’t include in the schematic don’t blow up; and there’s almost always a better way to do the job. OK, so I added another thing.

"You said two things," I reminded him. "Perhaps I did, but I added a third thing," he said before adding another thing. "Oh, one more thing: the crew safety and mission success requirements are very stringent, and the reliability of this particular circuit needs to be very, very high. We have an engineer on staff that’s done some 400 Hz magnetic, I’ll have him take a look."

Two weeks later I looked at his design. It used a transformer in a magnetic amplifier configuration, with its inductance modulated with a variable DC current through an auxiliary winding to keep its inductance tuned to the variable load capacitance. By resonating the load capacitance, the efficiency was much higher, and the parts count was much lower.

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About the author
Larry Baxter is an electronics engineer specialising in analogue circuit design with a BSEE from RPI (Rensselaer Polytechnic Institute, New York). He wrote the book on capacitive sensors (“Capacitive Sensors,” IEEE Press) and is a consultant for low-noise design and capacitive sensors.
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